FIG. 1

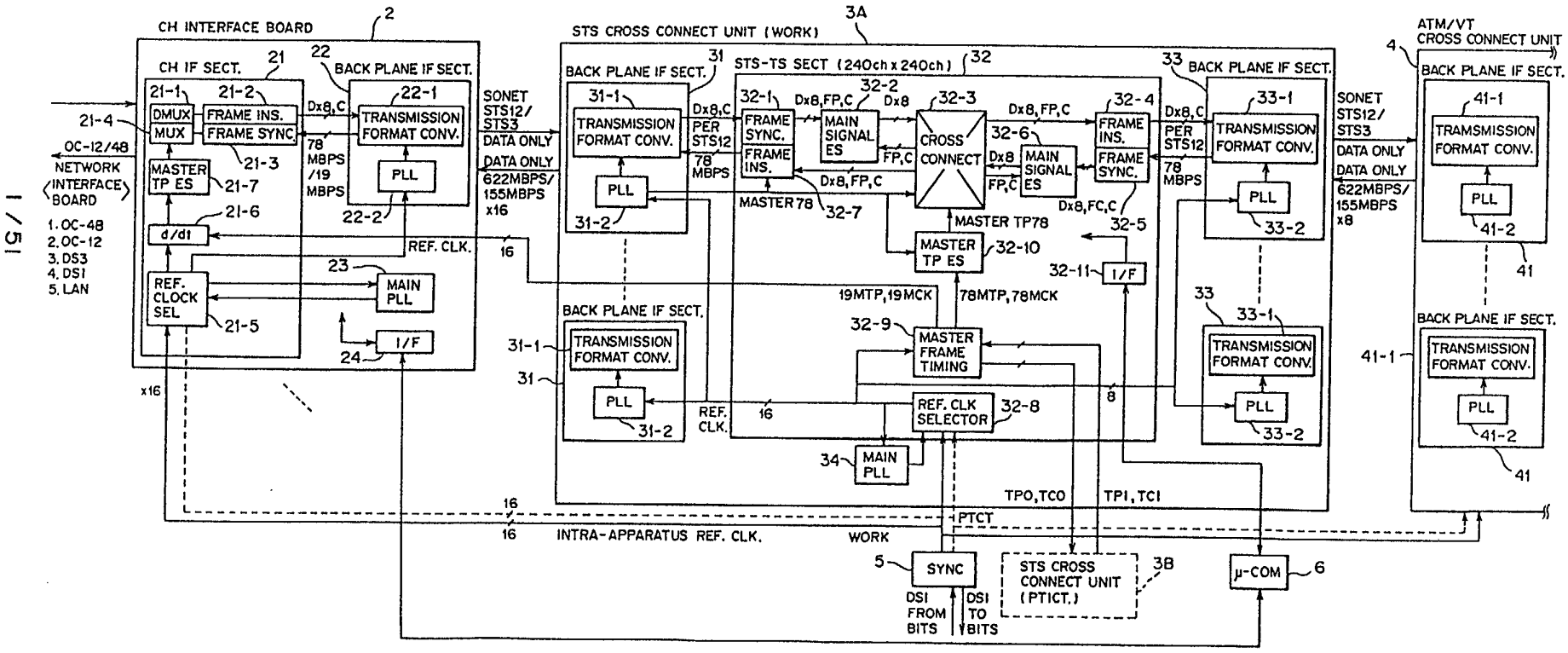


FIG. 2

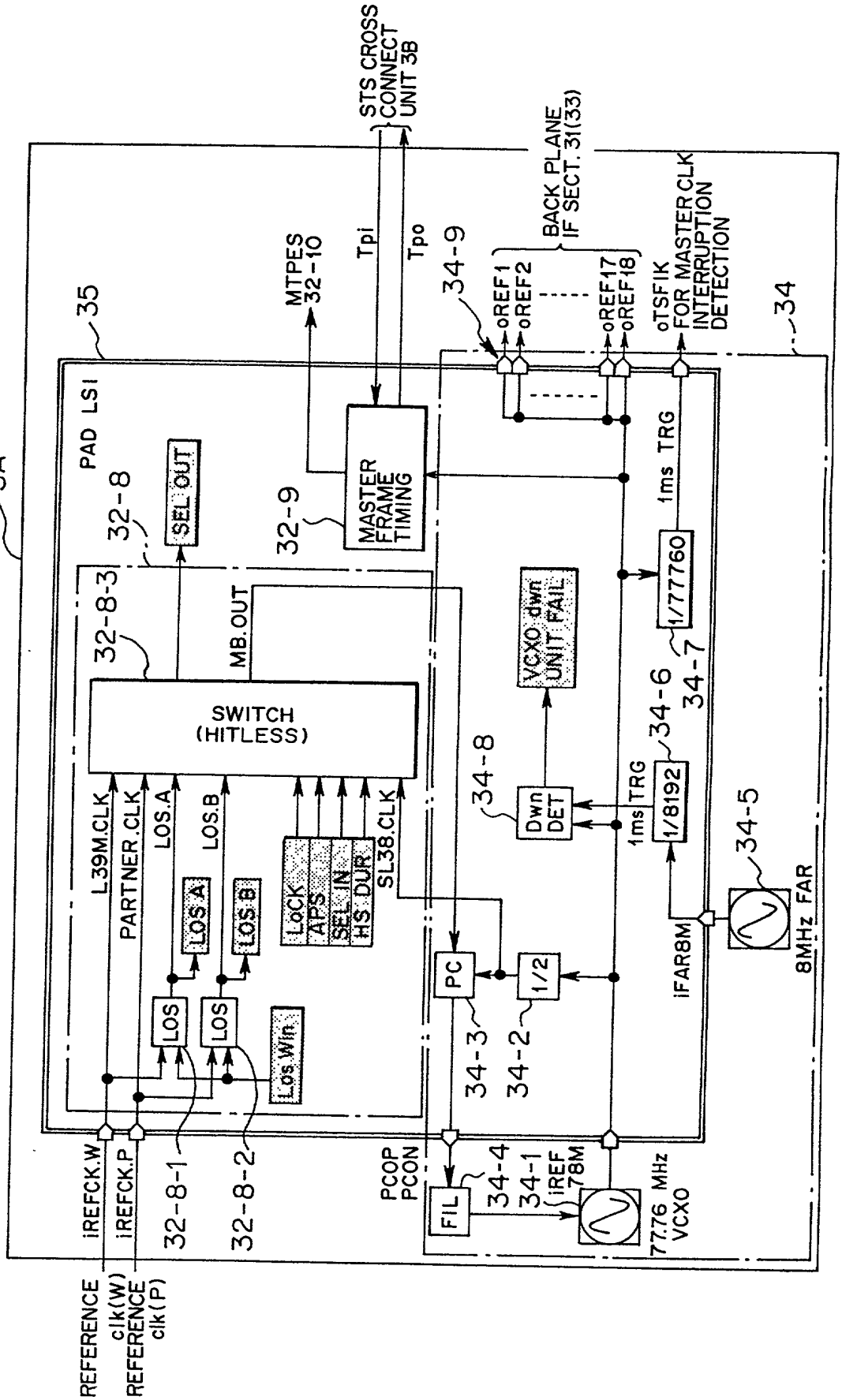


FIG. 3

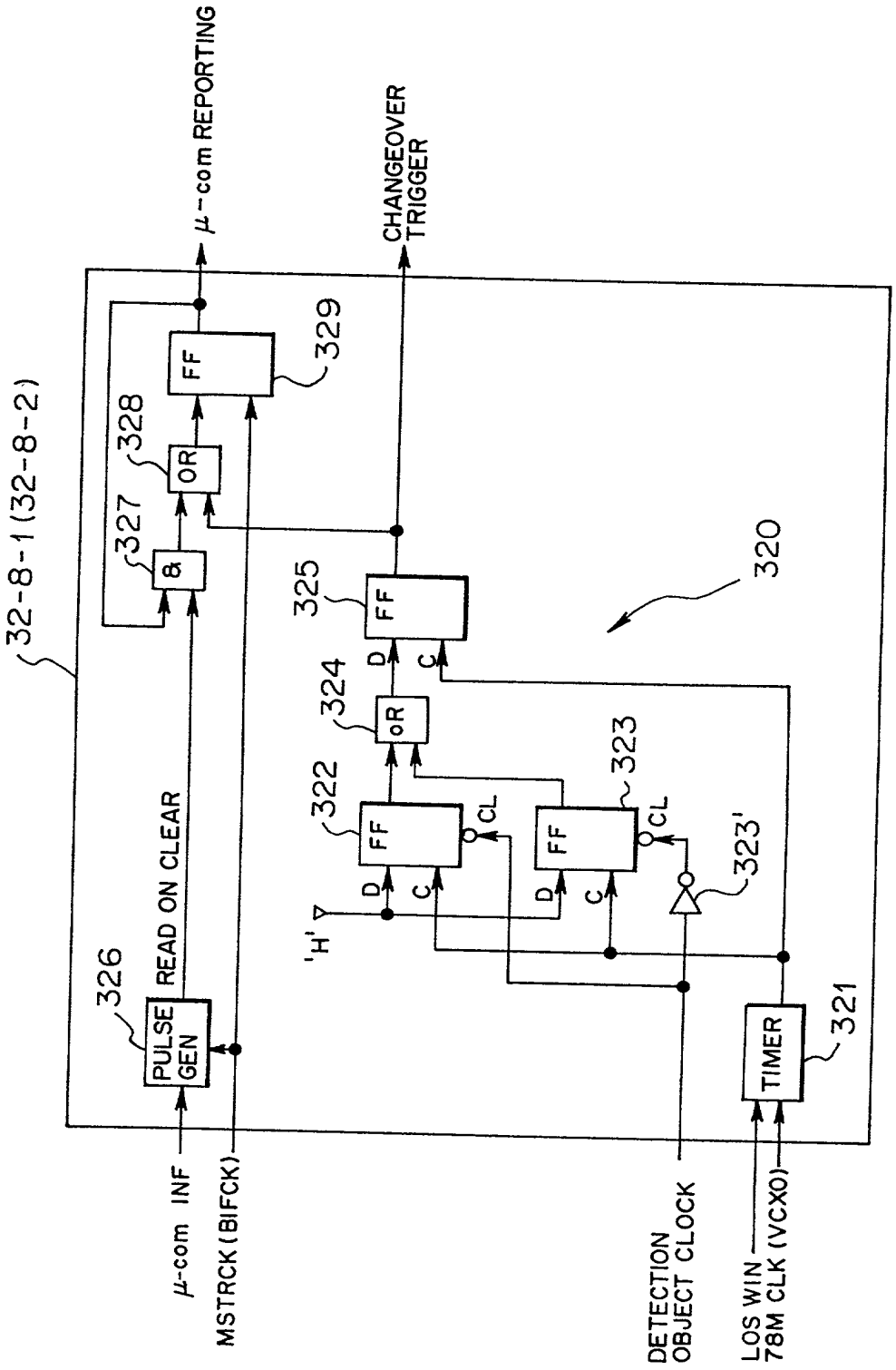


FIG. 4A

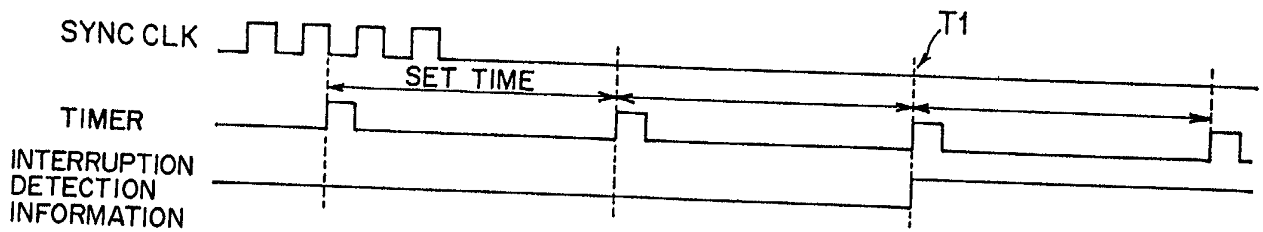

SYNC CLK
TIMER
INTERRUPTION DETECTION INFORMATION
SET TIME
T1

FIG. 4B

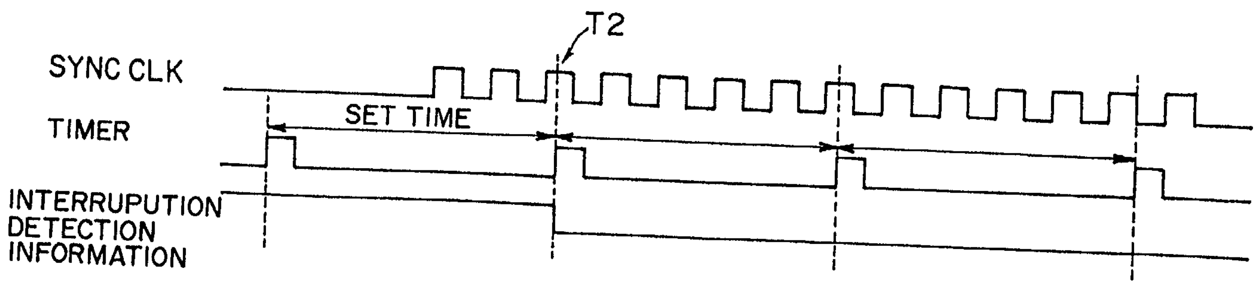

SYNC CLK
TIMER
INTERRUPUTION DETECTION INFORMATION
SET TIME
T2

FIG. 5

μ-com LOS WIN				WINDOW TIME	DIVIDING TIMER
D3	D2	D1	DO	(ns)	
0	0	0	0	25.7	77.76 M/4
0	0	0	1	77.2	77.76 M/8
0	0	1	0	128.6	77.76 M/12
0	0	1	1	180.7	77.76 M/16
0	1	0	0	231.5	77.76 M/20
0	1	0	1	282.9	77.76 M/24
0	1	1	0	334.3	77.76 M/28
0	1	1	1	385.8	77.76 M/32
1	0	0	0	437.3	77.76 M/36
1	0	0	1	488.7	77.76 M/40
1	0	1	0	540.1	77.76 M/44
1	0	1	1	591.6	77.76 M/48
1	1	0	0	643.0	77.76 M/52
1	1	0	1	694.5	77.76 M/56
1	1	1	0	745.9	77.76 M/60
1	1	1	1	797.3	77.76 M/64

FIG. 6

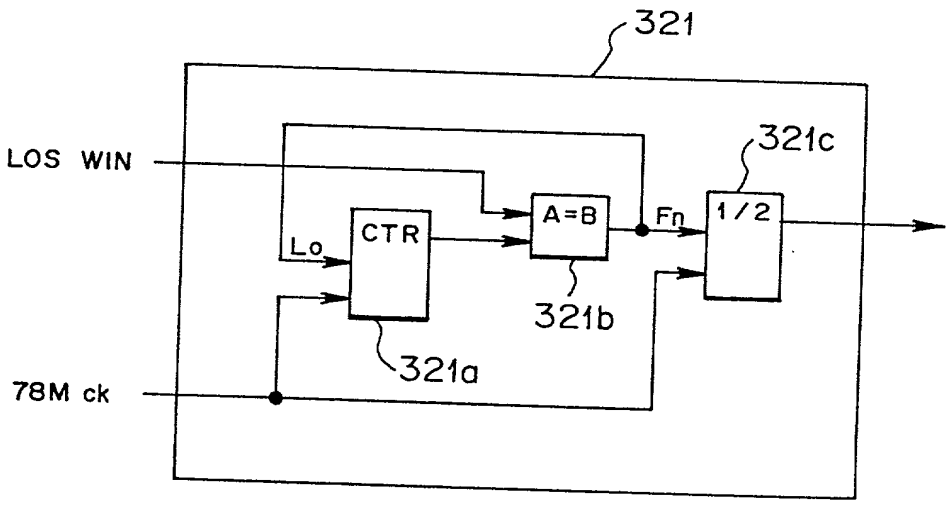


FIG. 7

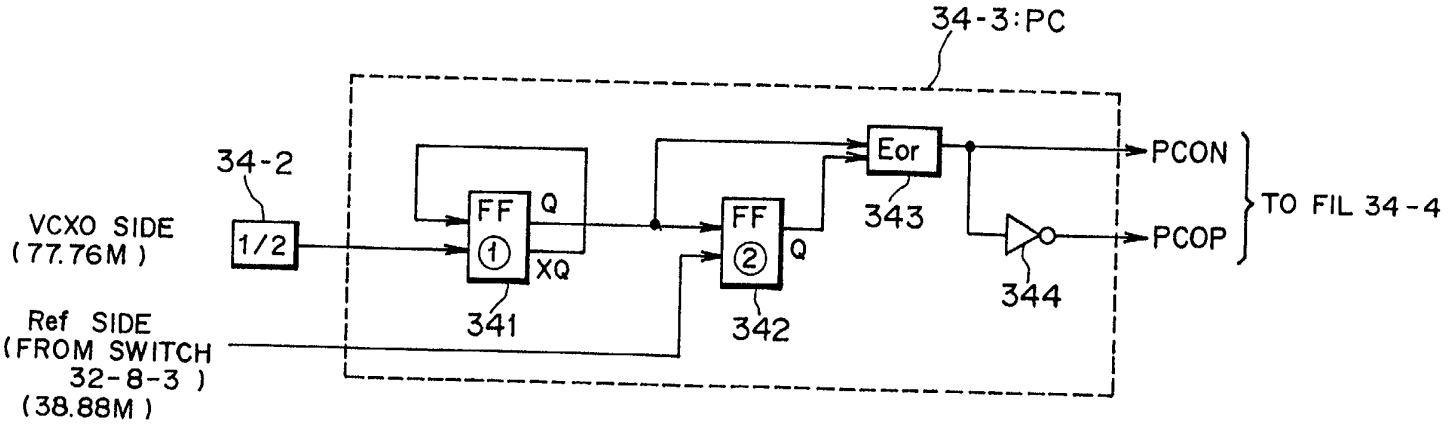

34-3:PC
34-2
VCXO SIDE
(77.76M)
1/2
Ref SIDE
(FROM SWITCH
32-8-3)
(38.88M)
FF
①
Q
XQ
341
FF
②
Q
342
Eor
343
344
PCON
PCOP
TO FIL 34-4

FIG.8A

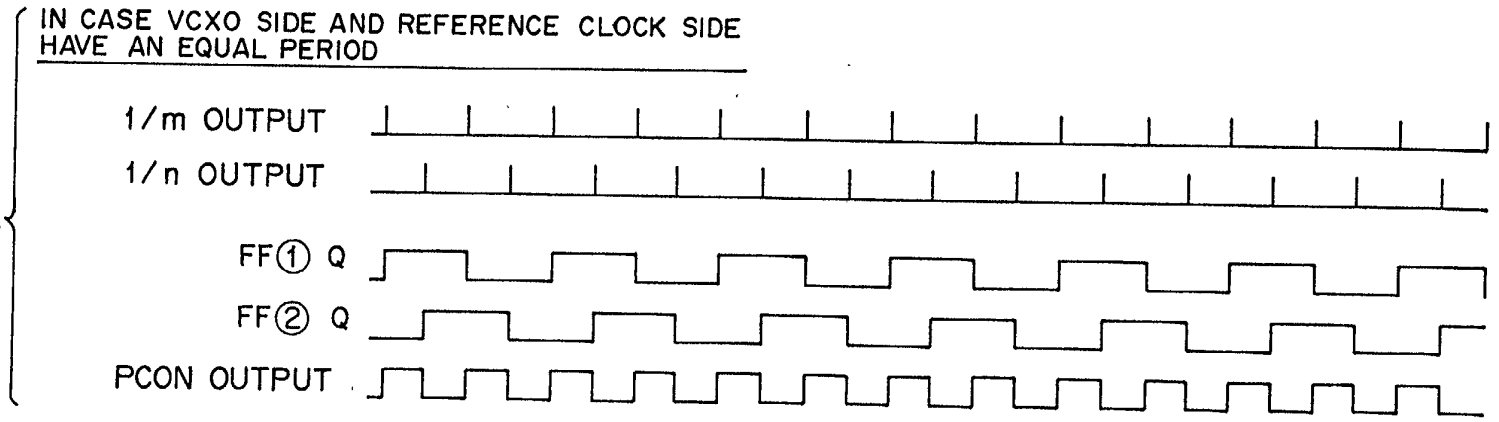

IN CASE VCXO SIDE AND REFERENCE CLOCK SIDE HAVE AN EQUAL PERIOD
1/m OUTPUT
1/n OUTPUT
FF① Q
FF② Q
PCON OUTPUT

FIG.8B

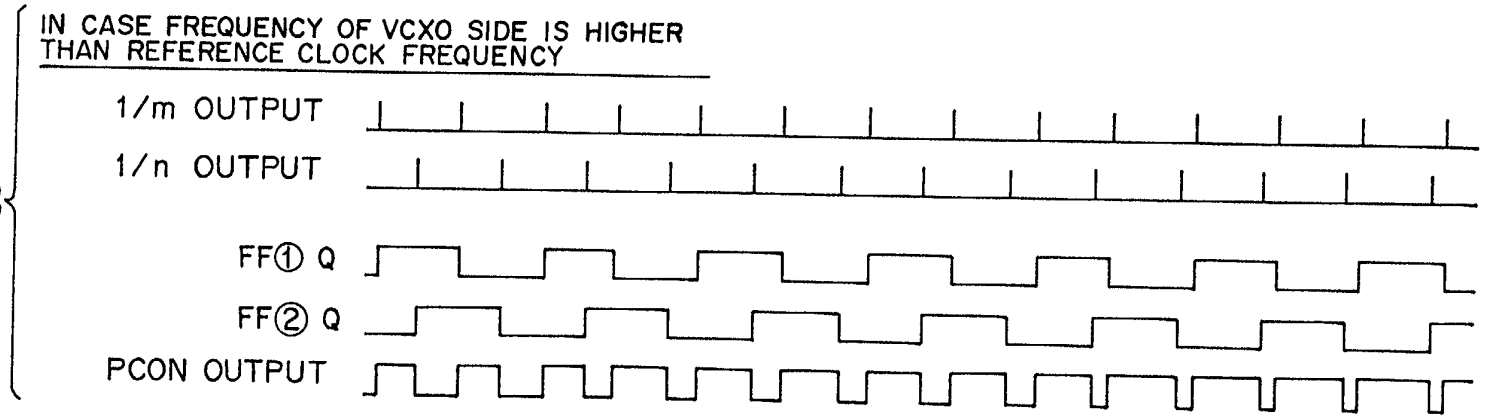

IN CASE FREQUENCY OF VCXO SIDE IS HIGHER THAN REFERENCE CLOCK FREQUENCY
1/m OUTPUT
1/n OUTPUT
FF① Q
FF② Q
PCON OUTPUT

FIG.9A

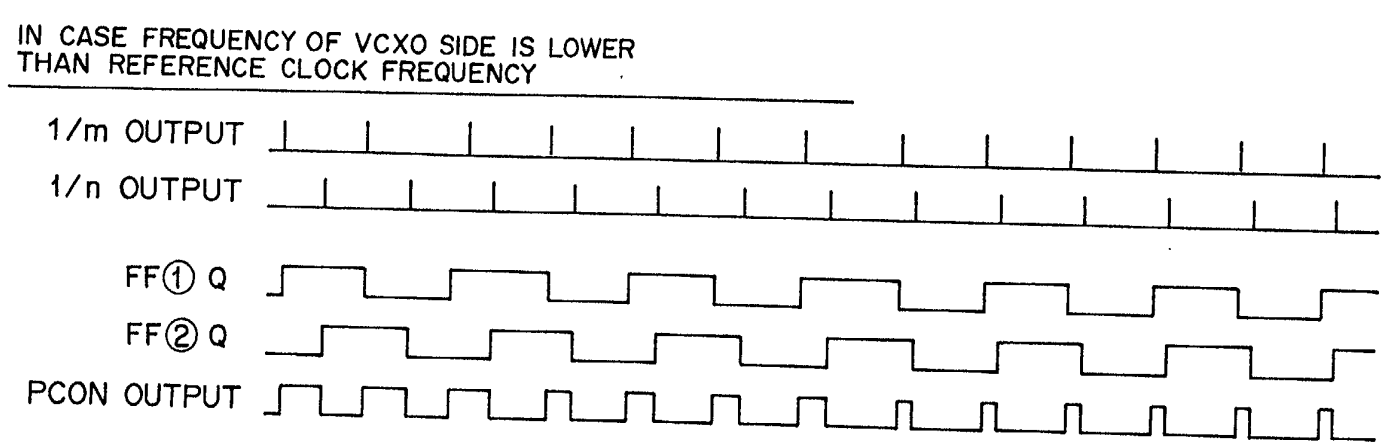

IN CASE FREQUENCY OF VCXO SIDE IS LOWER THAN REFERENCE CLOCK FREQUENCY
1/m OUTPUT
1/n OUTPUT
FF① Q
FF② Q
PCON OUTPUT

FIG.9B

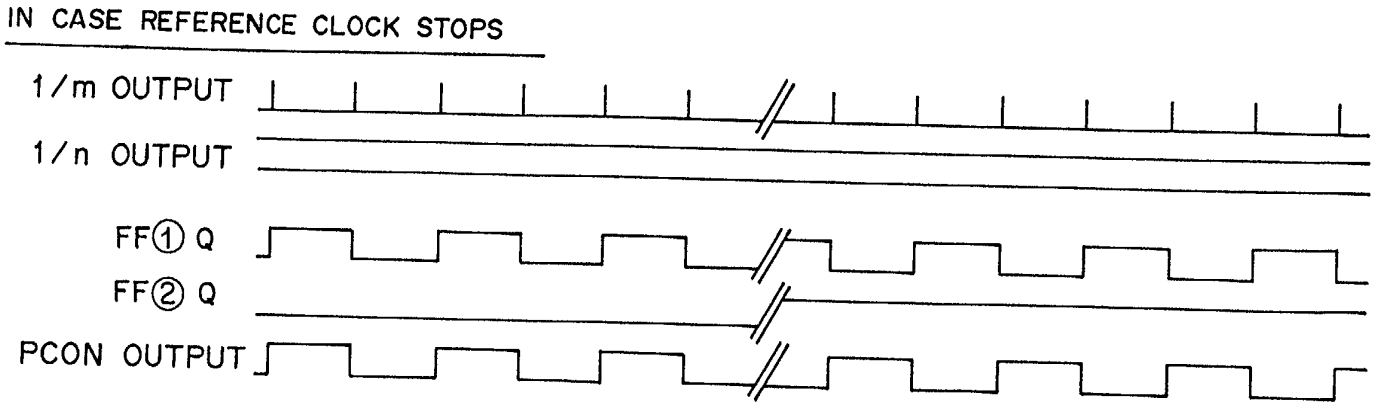

IN CASE REFERENCE CLOCK STOPS
1/m OUTPUT
1/n OUTPUT
FF① Q
FF② Q
PCON OUTPUT

FIG. 10

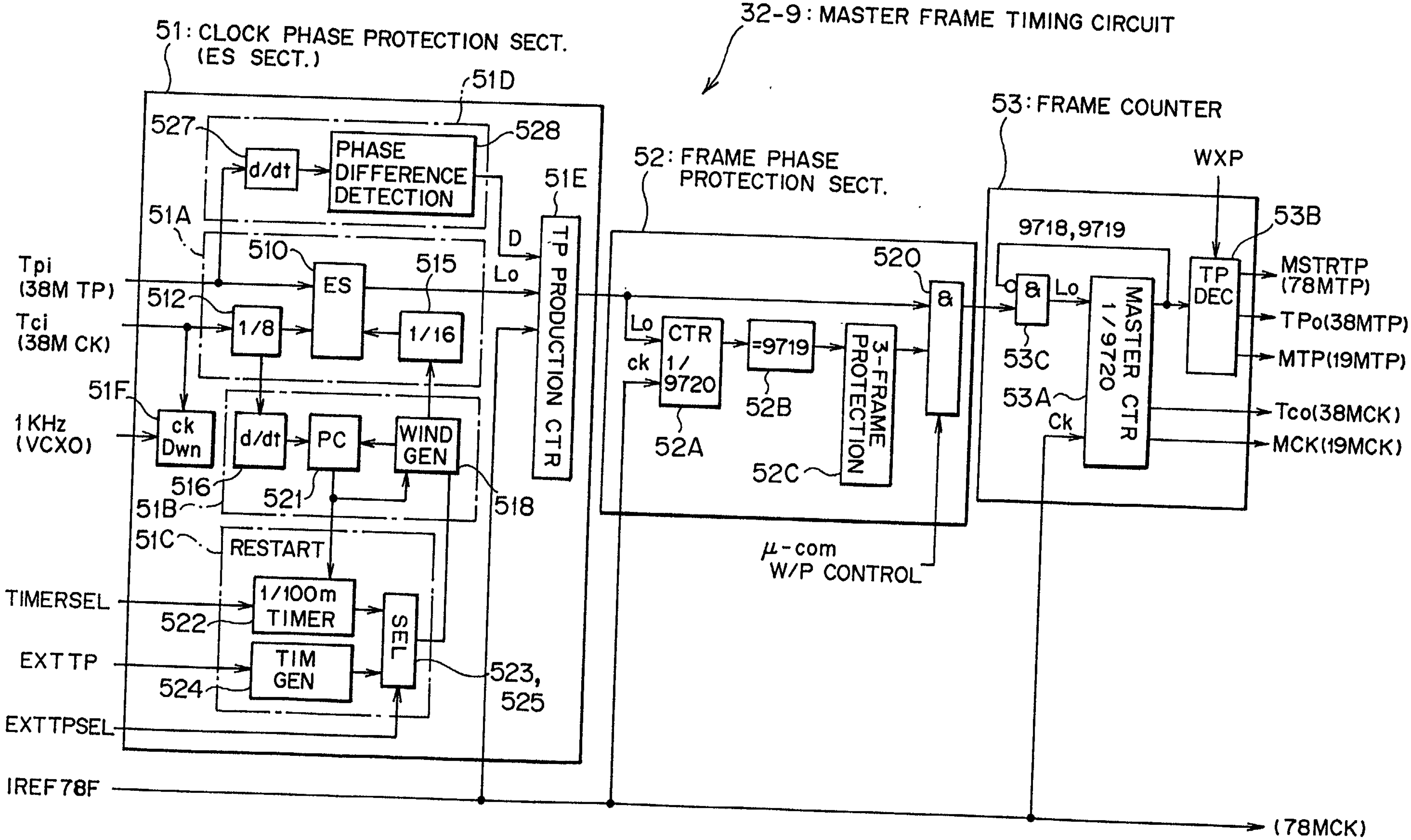

32-9 : MASTER FRAME TIMING CIRCUIT
51 : CLOCK PHASE PROTECTION SECT. (ES SECT.)
51D
527
d/dt
PHASE DIFFERENCE DETECTION
528
51A
510
ES
515
1/16
512
1/8
Tpi (38M TP)
Tci (38M CK)
51F
1 KHz (VCXO)
ck Dwn
d/dt
PC
WIND GEN
516
521
51B
518
51C
RESTART
1/100m TIMER
TIM GEN
SEL
522
524
523, 525
TIMERSEL
EXTTP
EXTTPSEL
IREF78F
51E
D
Lo
TP PRODUCTION CTR
52 : FRAME PHASE PROTECTION SECT.
Lo
ck
CTR 1/ 9720
52A
=9719
52B
3-FRAME PROTECTION
52C
520
&
μ-com W/P CONTROL
53 : FRAME COUNTER
9718, 9719
&
Lo
53C
MASTER CTR 1/9720
53A
Ck
WXP
TP DEC
53B
MSTRTP (78MTP)
TPo(38MTP)
MTP(19MTP)
Tco(38MCK)
MCK(19MCK)
(78MCK)

FIG. 11

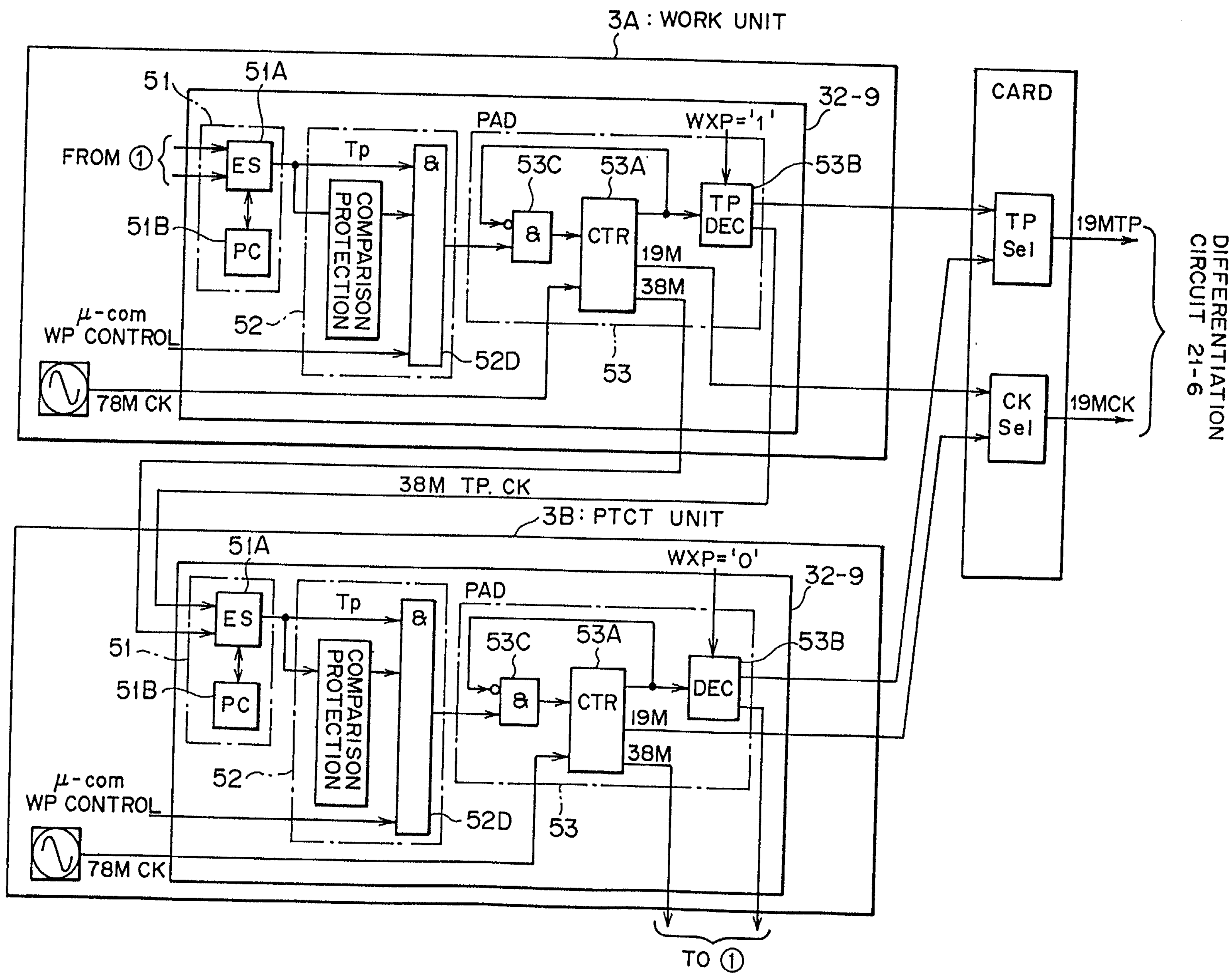

3A : WORK UNIT
51
51A
FROM ①
ES
51B
PC
Tp
COMPARISON PROTECTION
&
52
52D
μ-com
WP CONTROL
78M CK
PAD
53C
53A
&
CTR
19M
38M
WXP='1'
TP DEC
53B
53
32-9
CARD
TP Sel
CK Sel
19MTP
19MCK
DIFFERENTIATION CIRCUIT 21-6
38M TP. CK
3B : PTCT UNIT
51A
ES
51
51B
PC
Tp
COMPARISON PROTECTION
&
52
52D
μ-com
WP CONTROL
78M CK
PAD
53C
53A
&
CTR
19M
38M
WXP='0'
DEC
53B
53
32-9
TO ①

FIG. 12

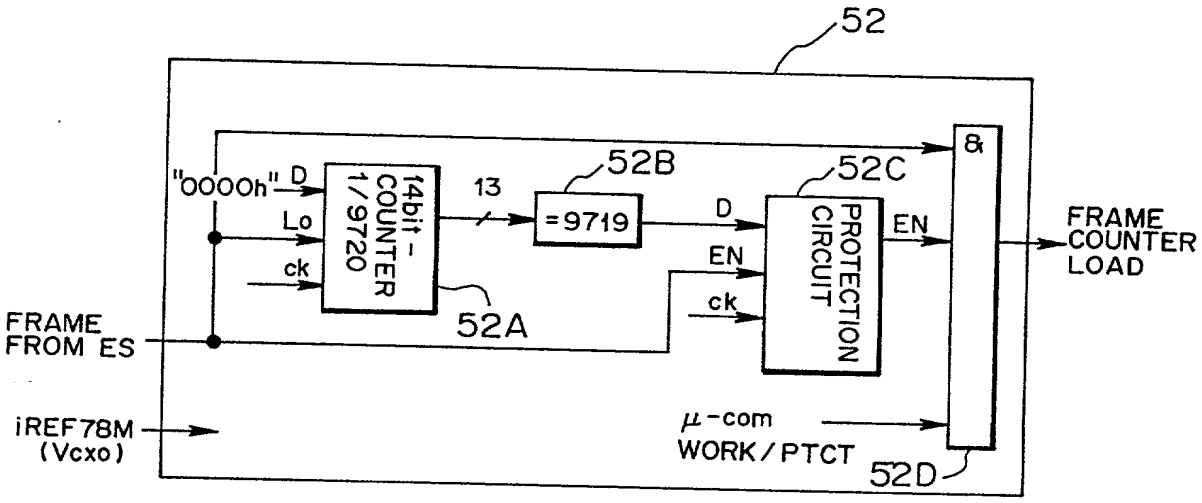

52
"0000h"
D
Lo
ck
14bit-COUNTER 1/9720
13
52B
=9719
52C
D
EN
ck
PROTECTION CIRCUIT
EN
&
FRAME COUNTER LOAD
52A
FRAME FROM ES
iREF78M (Vcxo)
μ-com WORK/PTCT
52D

FIG. 13

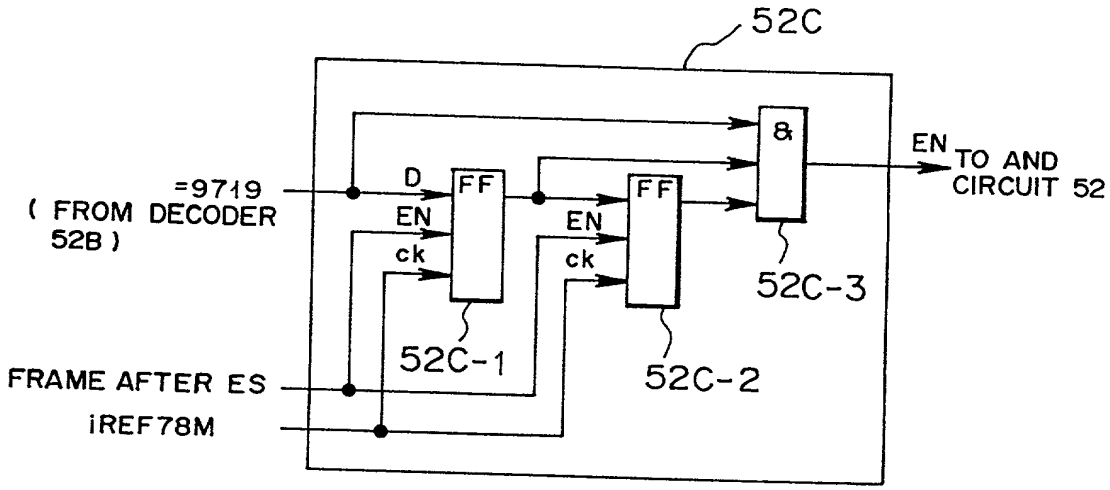

52C
=9719 (FROM DECODER 52B)
D
EN
ck
FF
52C-1
FF
52C-2
&
52C-3
EN TO AND CIRCUIT 52
FRAME AFTER ES
iREF78M

FIG. 14A

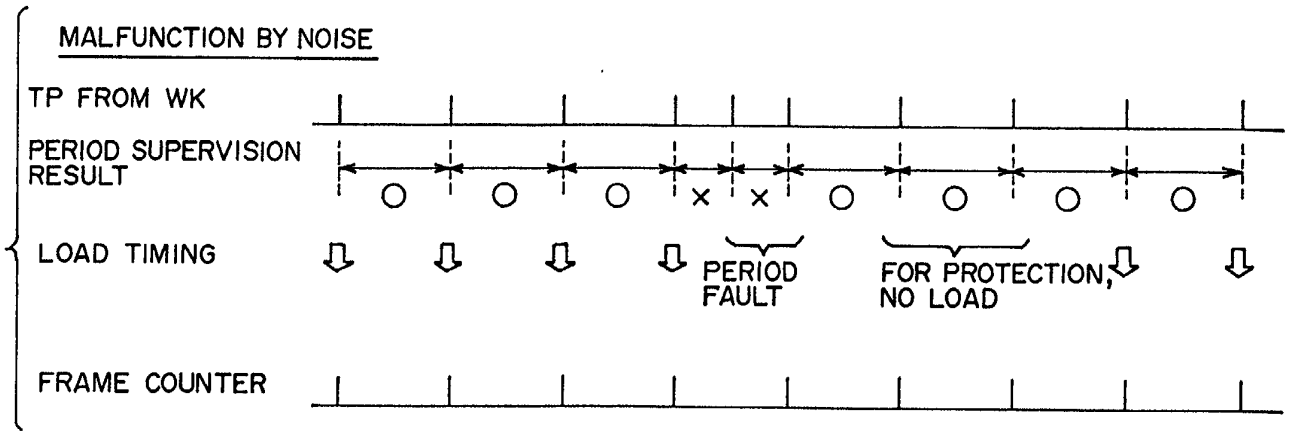


FIG. 14B

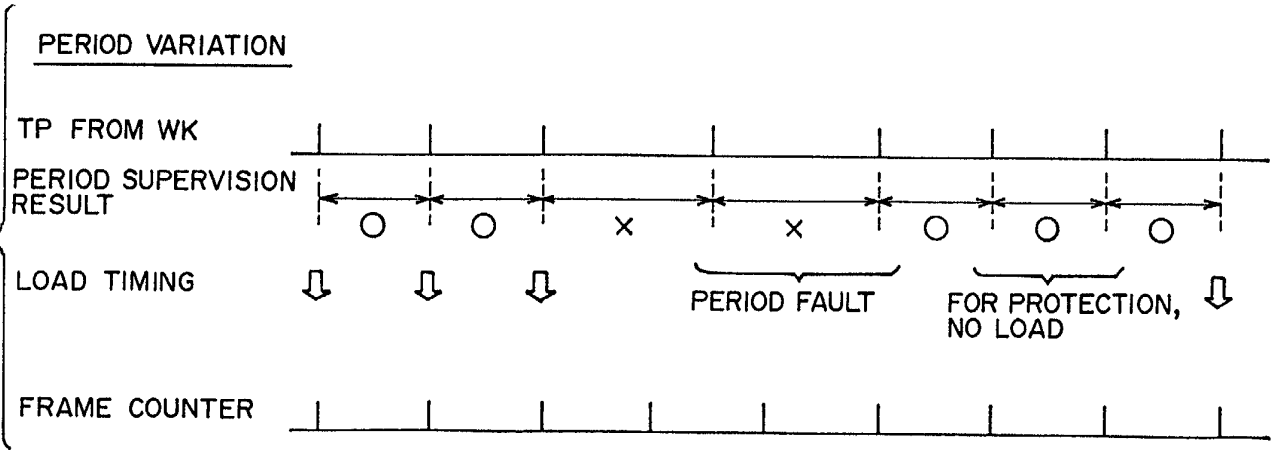


FIG. 15

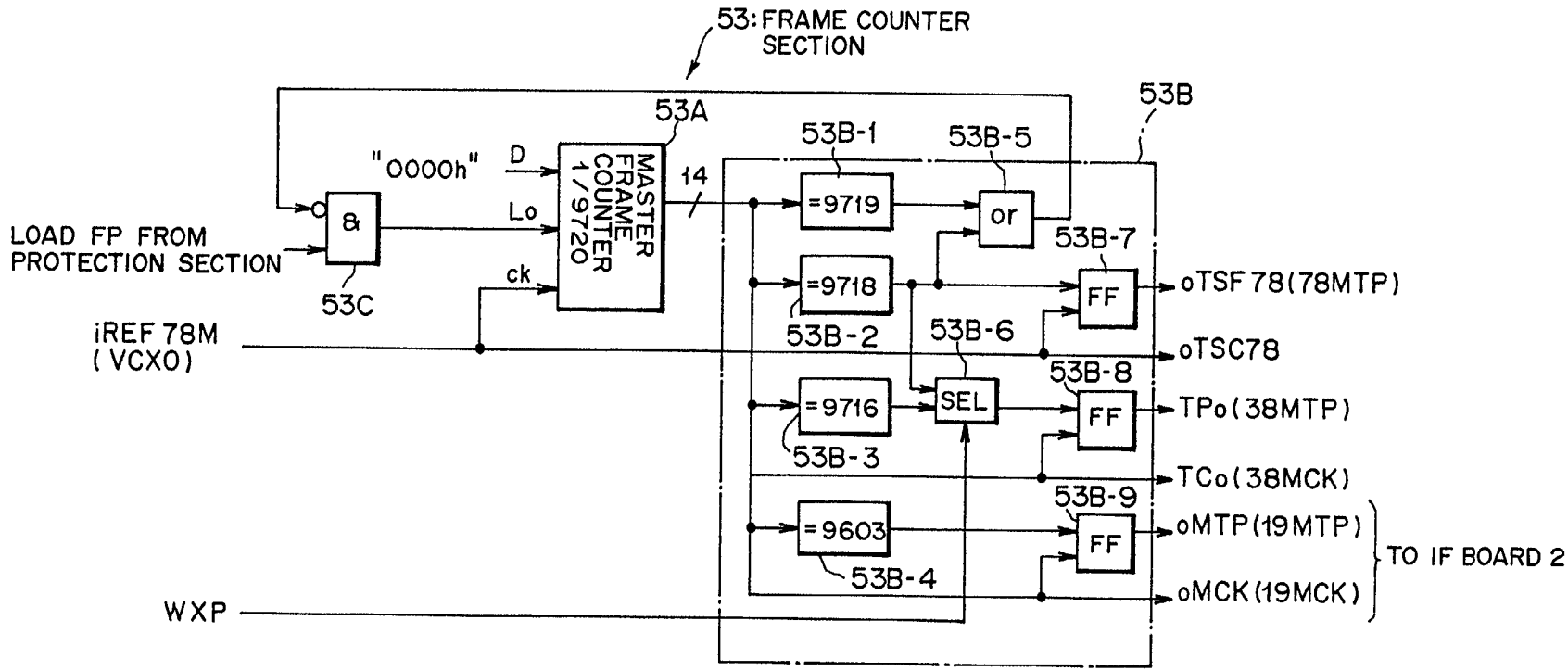

53: FRAME COUNTER SECTION
53A
53B
53B-1
53B-5
"0000h"
D
Lo
ck
14
MASTER FRAME COUNTER 1/9720
&
53C
LOAD FP FROM PROTECTION SECTION
iREF 78M (VCXO)
=9719
or
53B-7
=9718
FF
oTSF 78 (78MTP)
53B-2
53B-6
oTSC78
53B-8
=9716
SEL
FF
TPo (38MTP)
53B-3
TCo (38MCK)
53B-9
=9603
FF
oMTP (19MTP)
53B-4
oMCK (19MCK)
TO IF BOARD 2
WXP

FIG. 16A

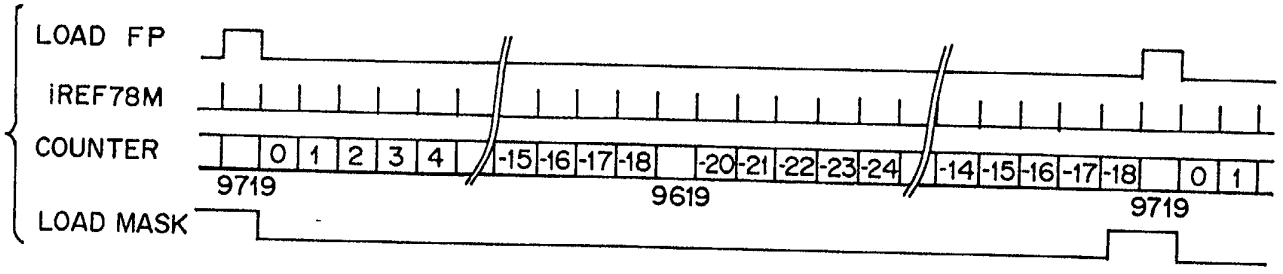


FIG. 16B

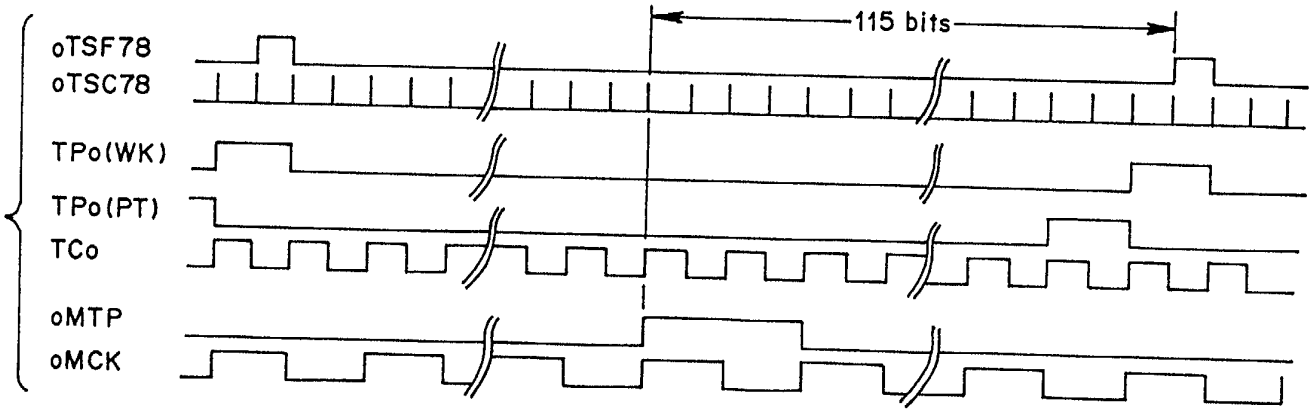
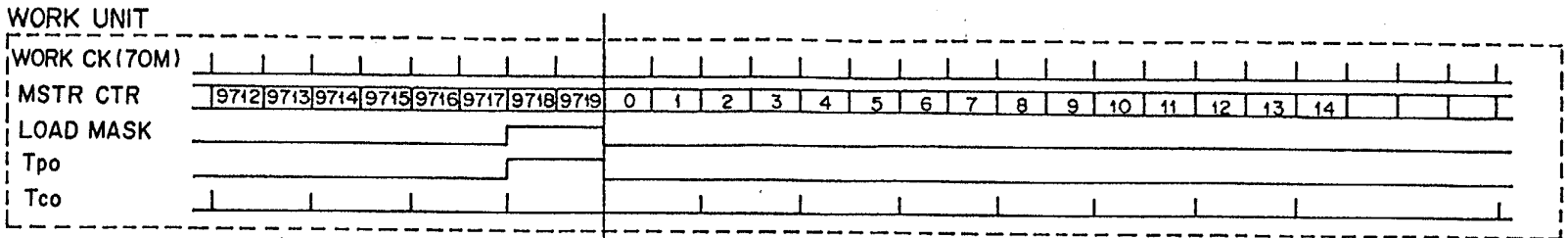


FIG.17A



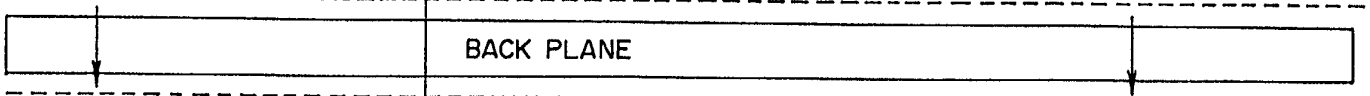
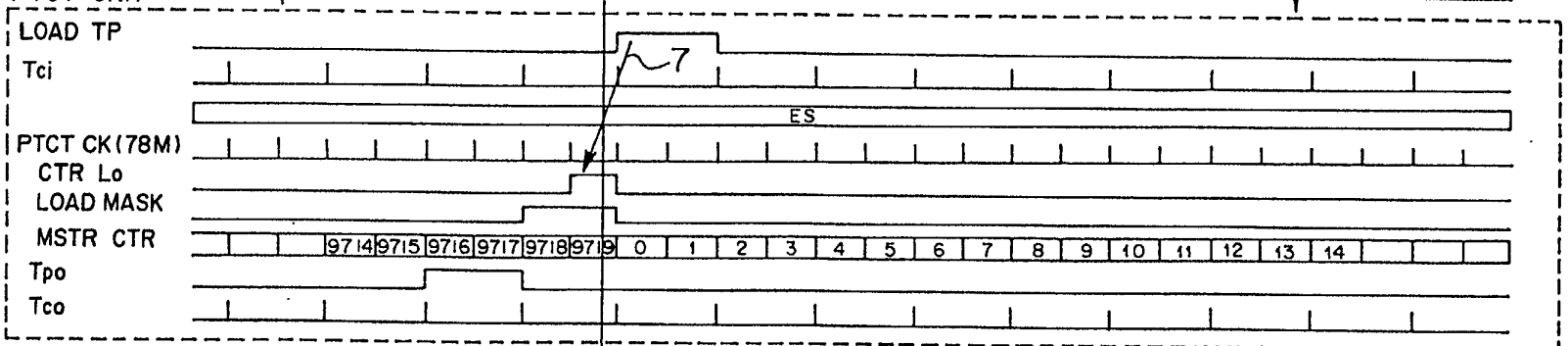


FIG.17B



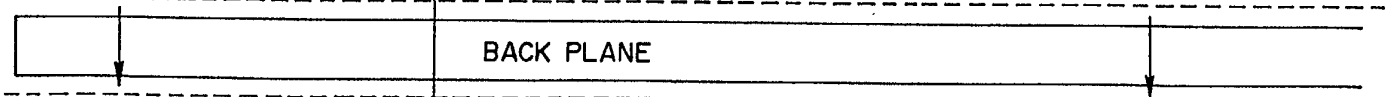


FIG.17C

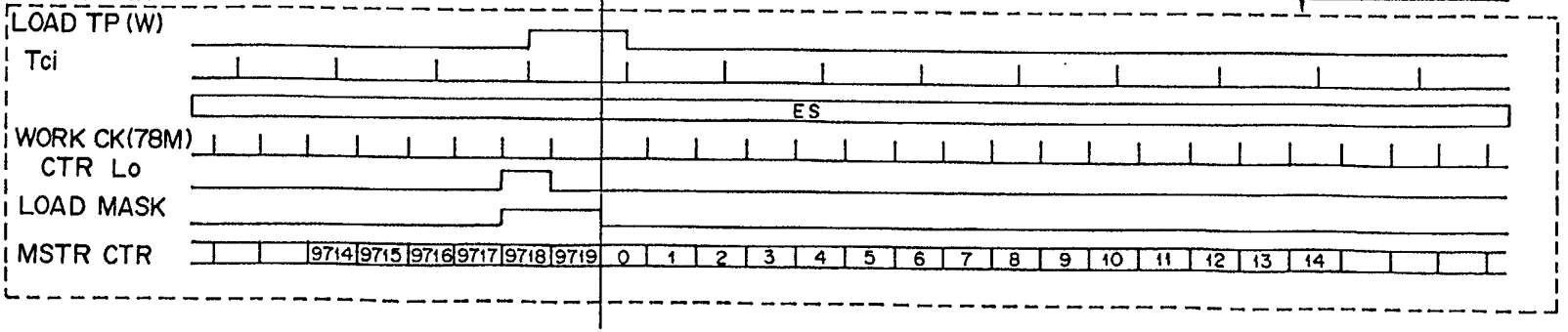


FIG.18

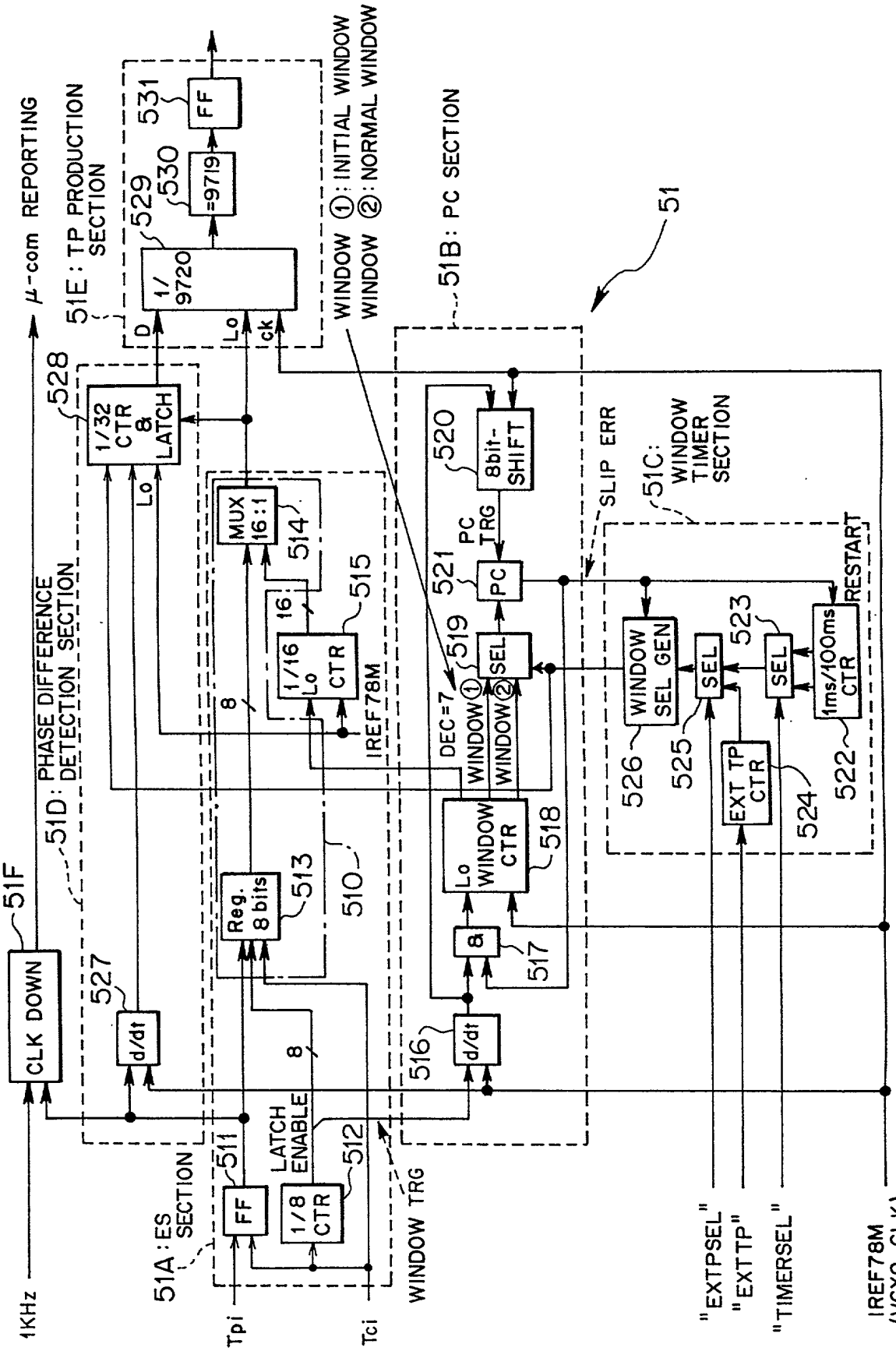


FIG. 19

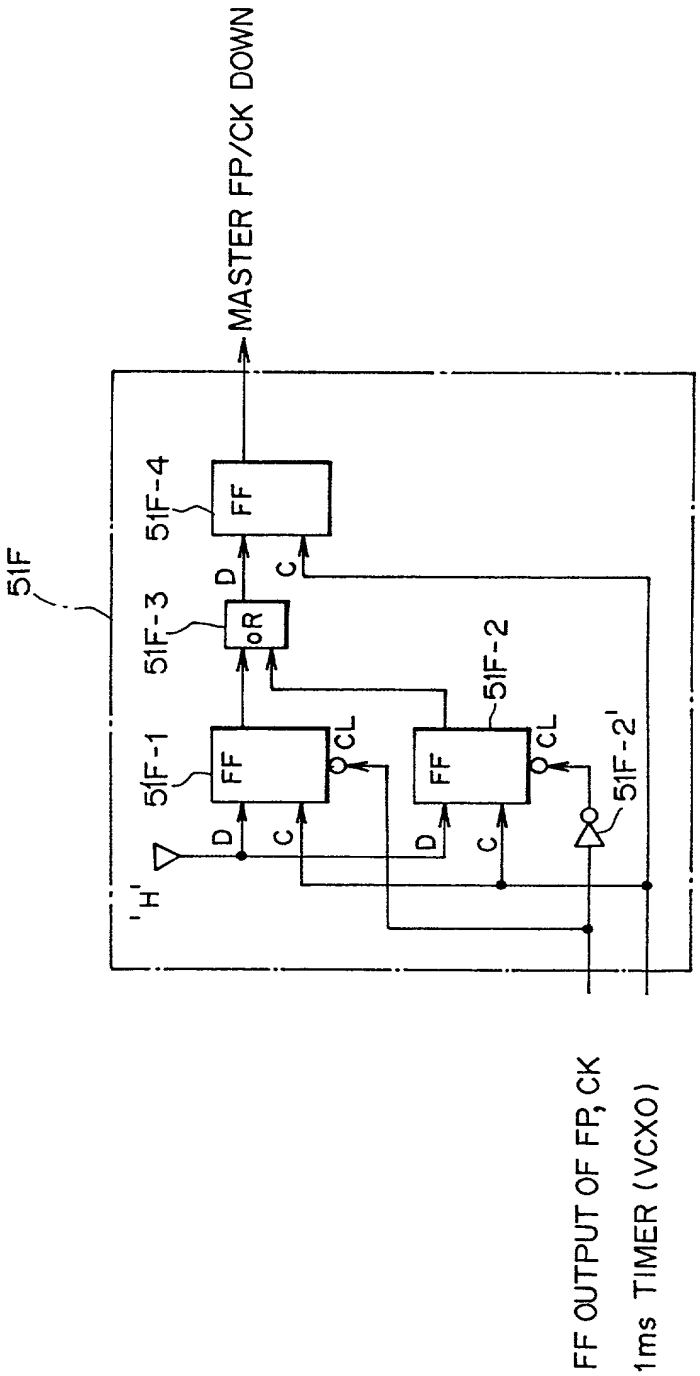


FIG. 20

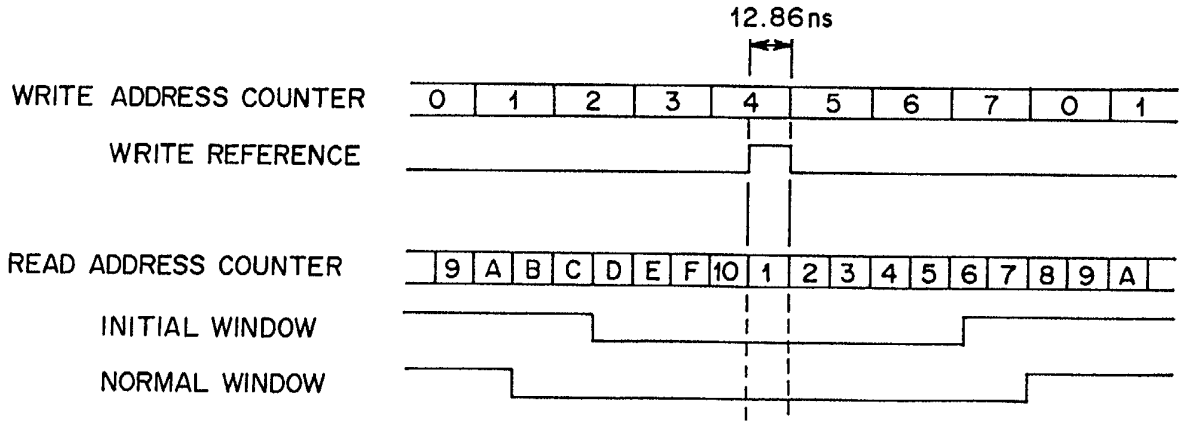
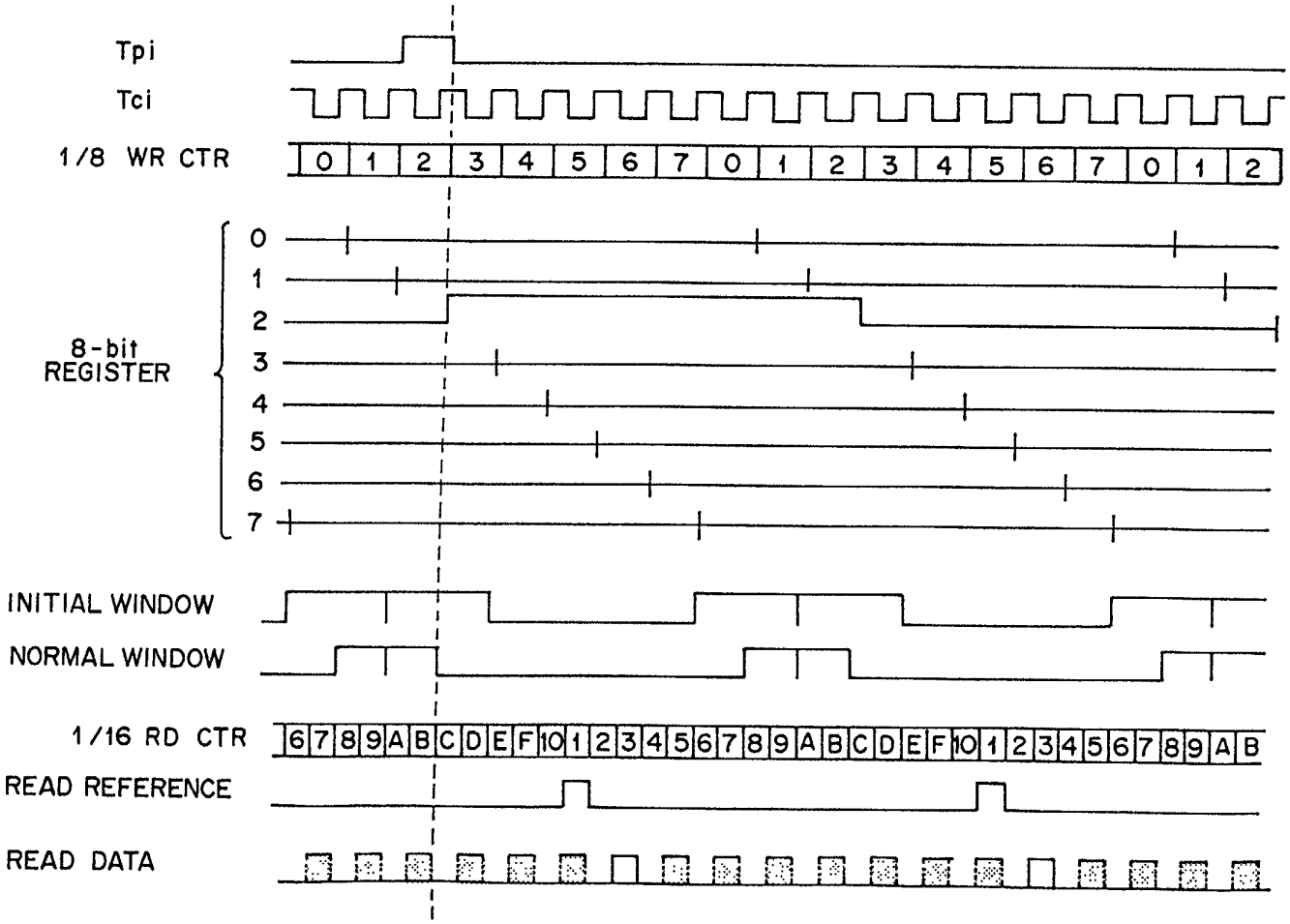


FIG. 21


Tpi
Tci
1/8 WR CTR
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2
8-bit REGISTER
0
1
2
3
4
5
6
7
INITIAL WINDOW
NORMAL WINDOW
1/16 RD CTR
6 7 8 9 A B C D E F 10 1 2 3 4 5 6 7 8 9 A B C D E F 10 1 2 3 4 5 6 7 8 9 A B
READ REFERENCE
READ DATA

[INTERNAL TIMER (1 ms/100ms)]

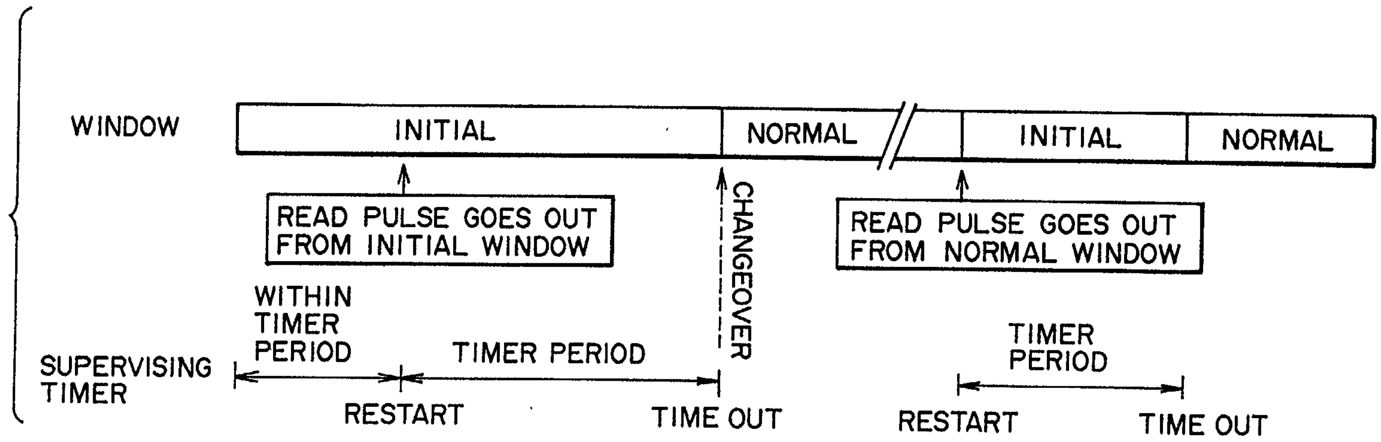


FIG. 22A

[EXTERNAL TIMER (EXT TP)]

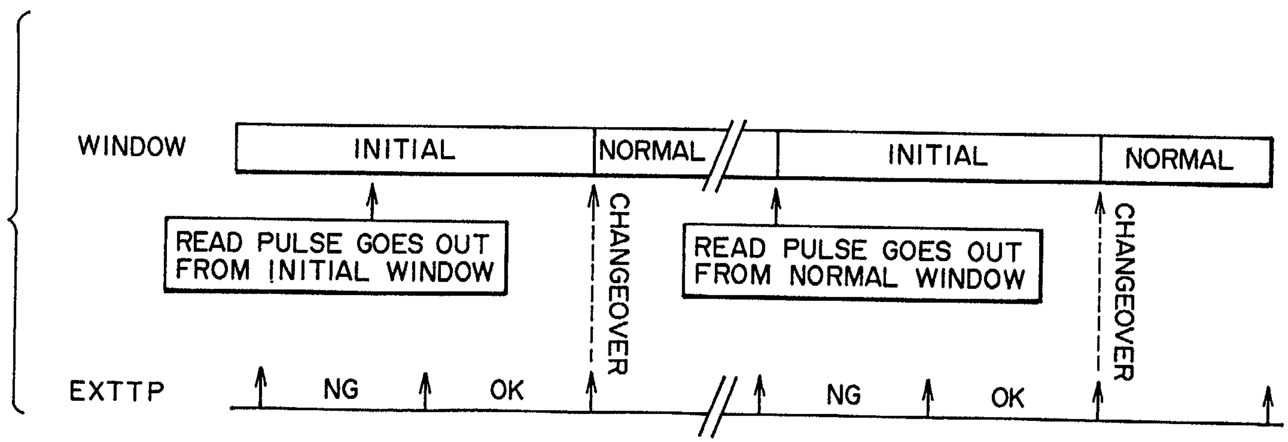


FIG. 22B

FIG. 23

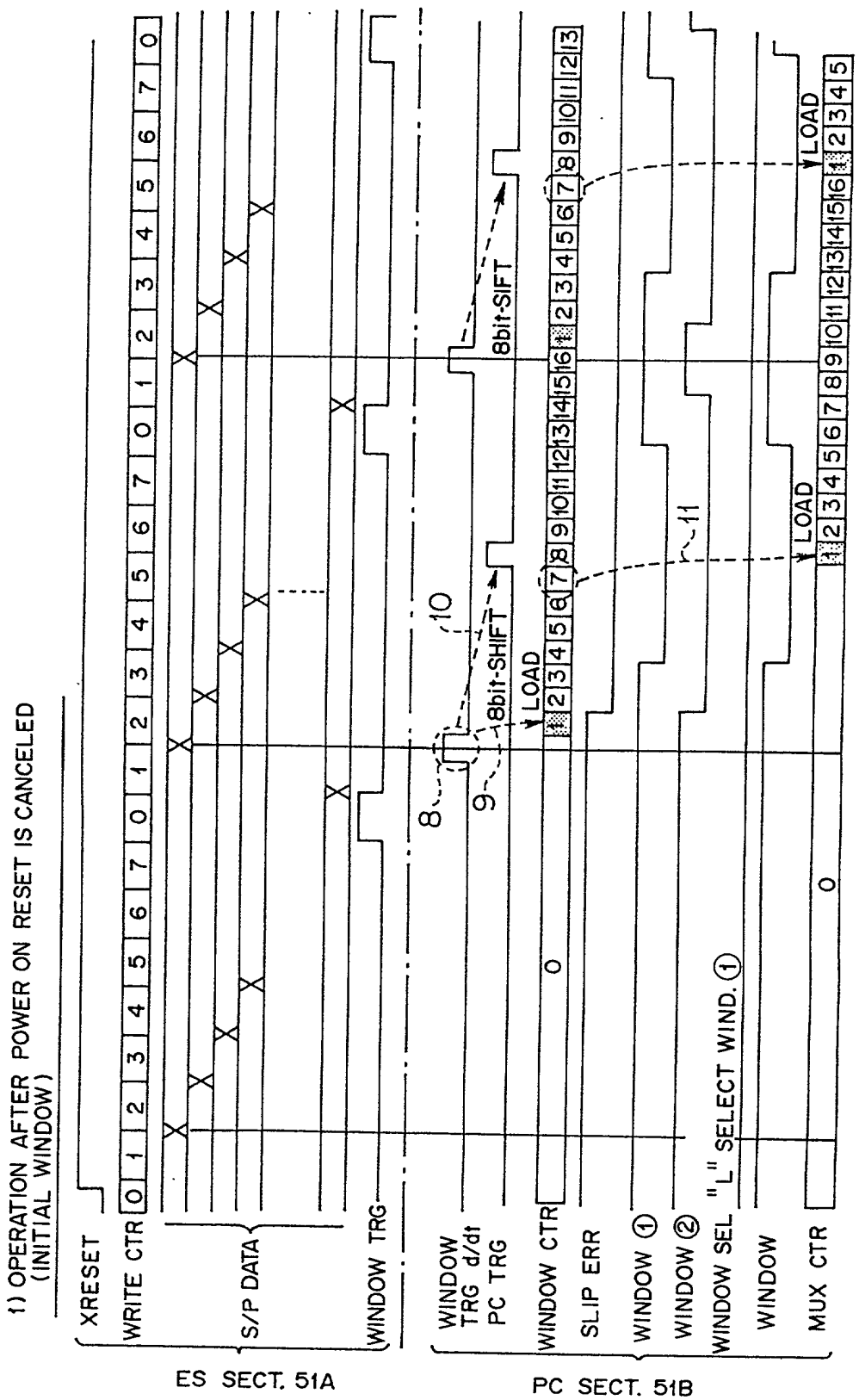


FIG. 24

2) OPERATION FOR CANCELLATION AFTER 1ms PROTECTION
(INITIAL WINDOW ⟶ NORMAL WINDOW)

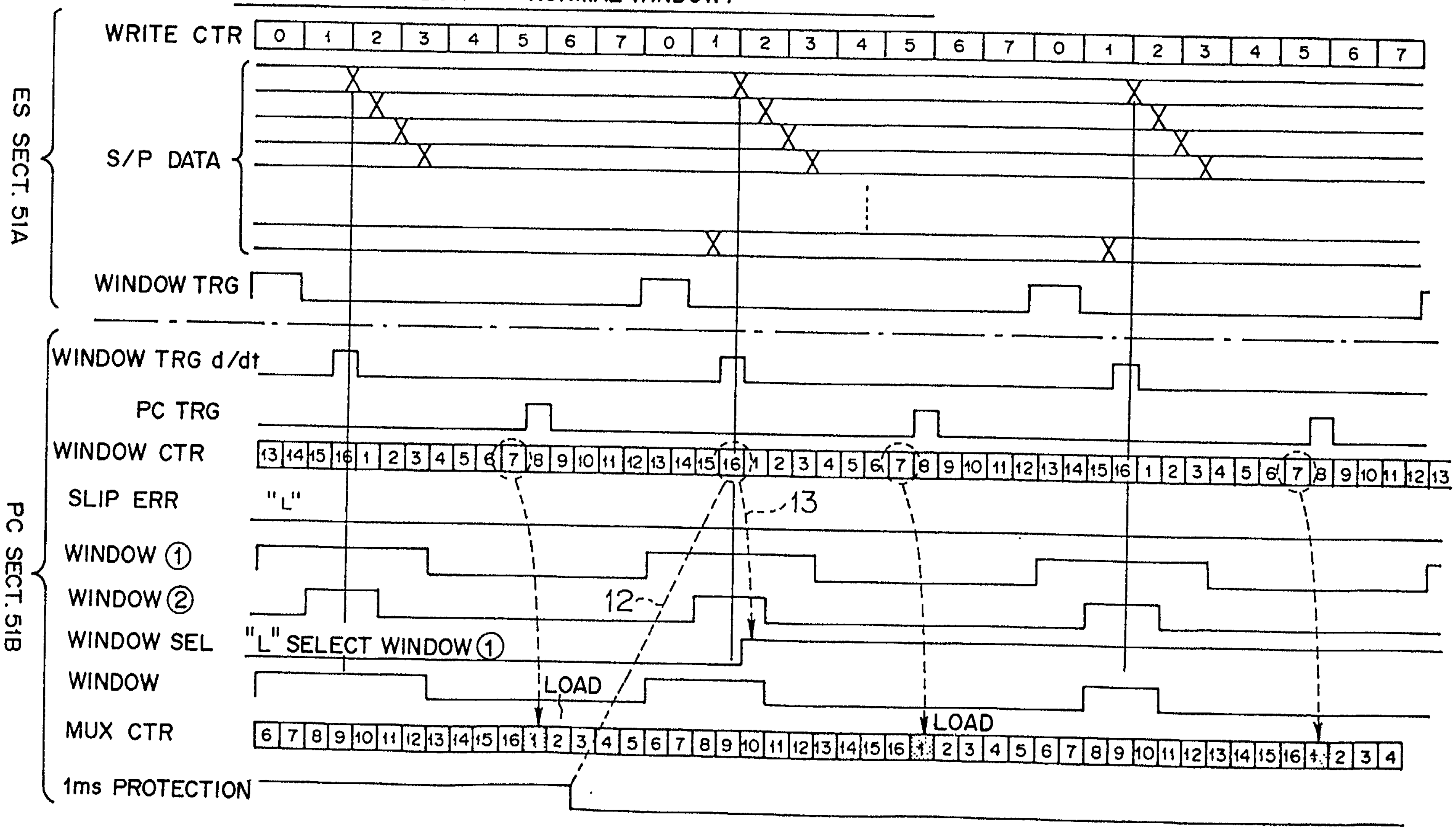


FIG. 25

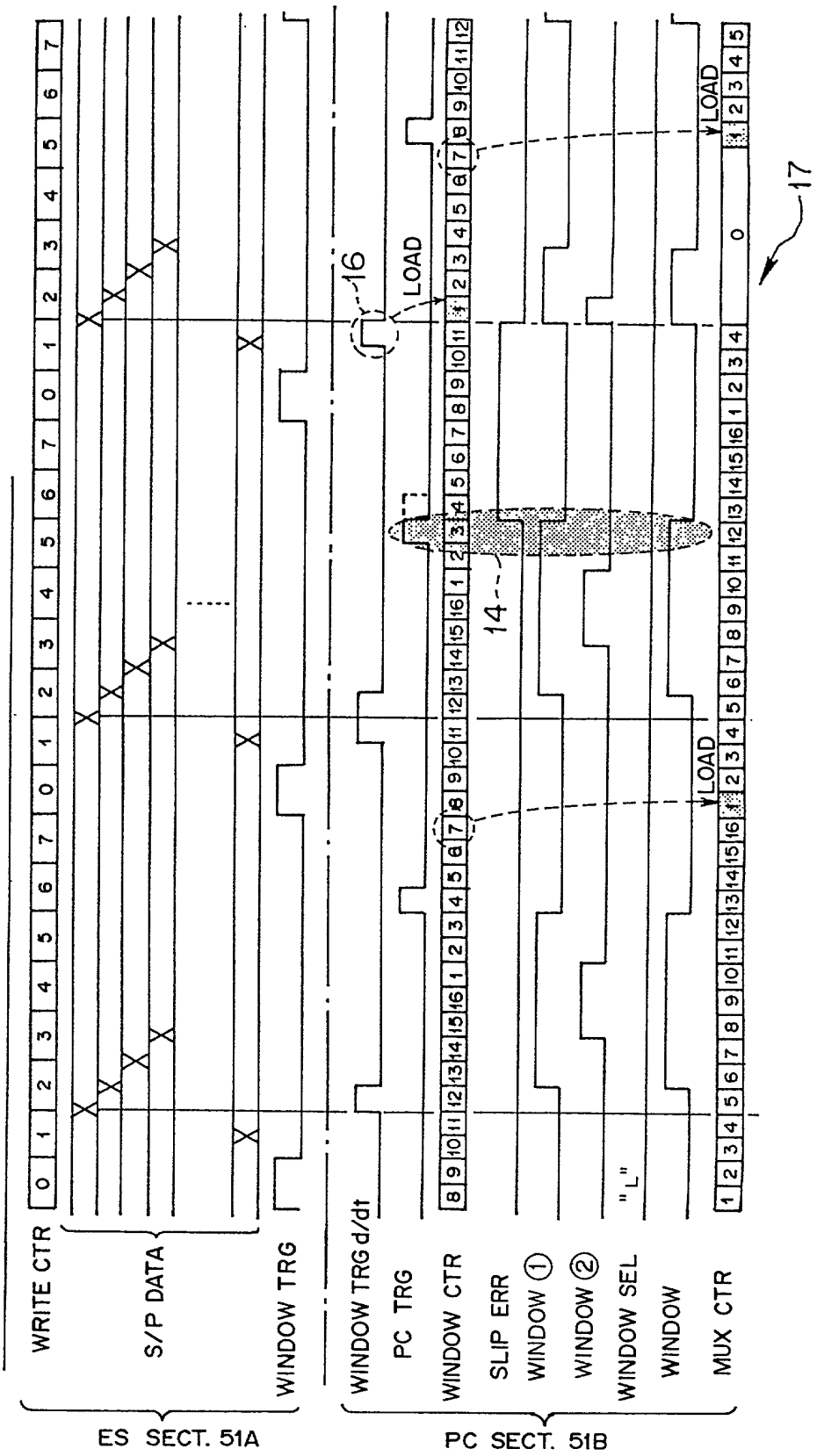


FIG. 26

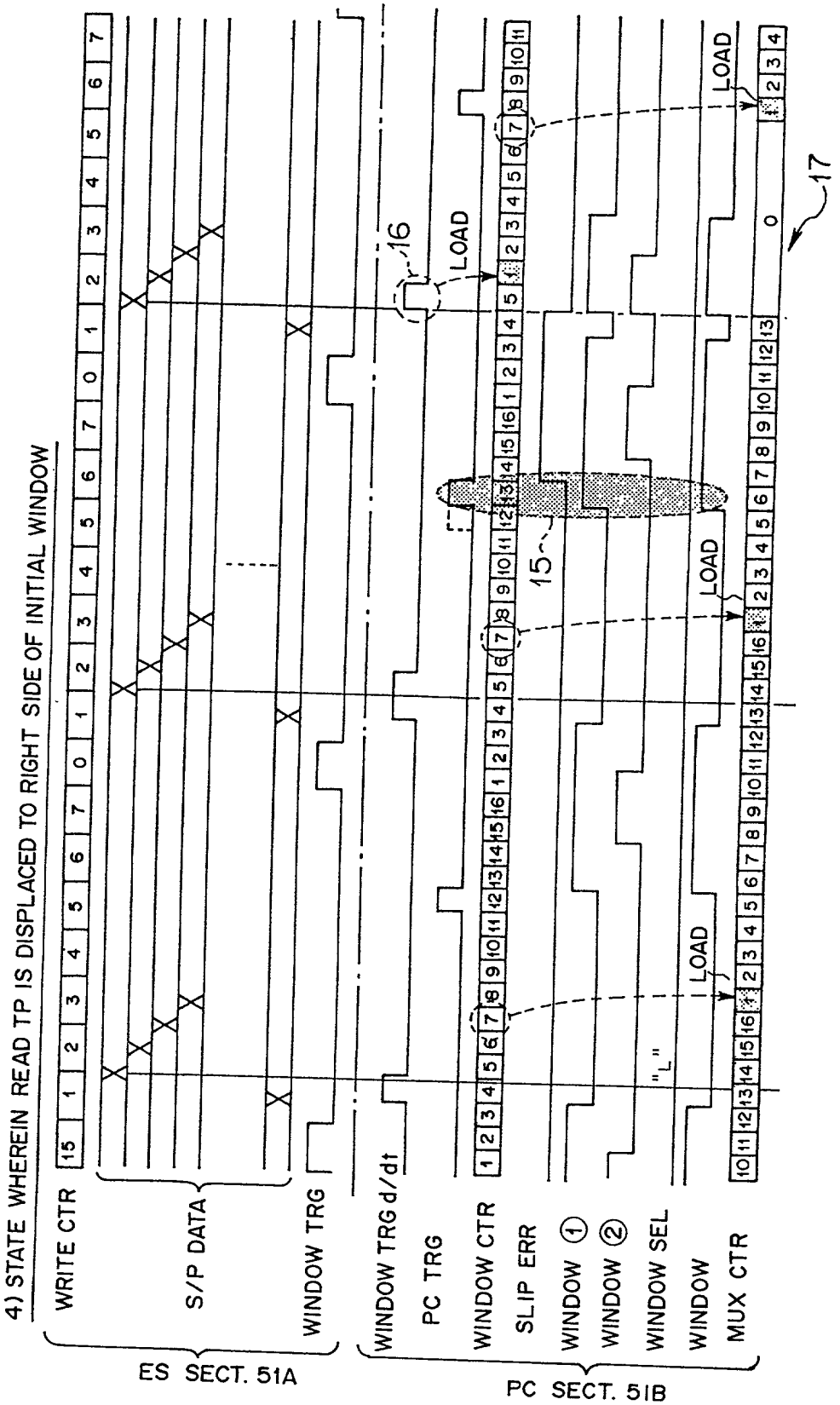


FIG. 27

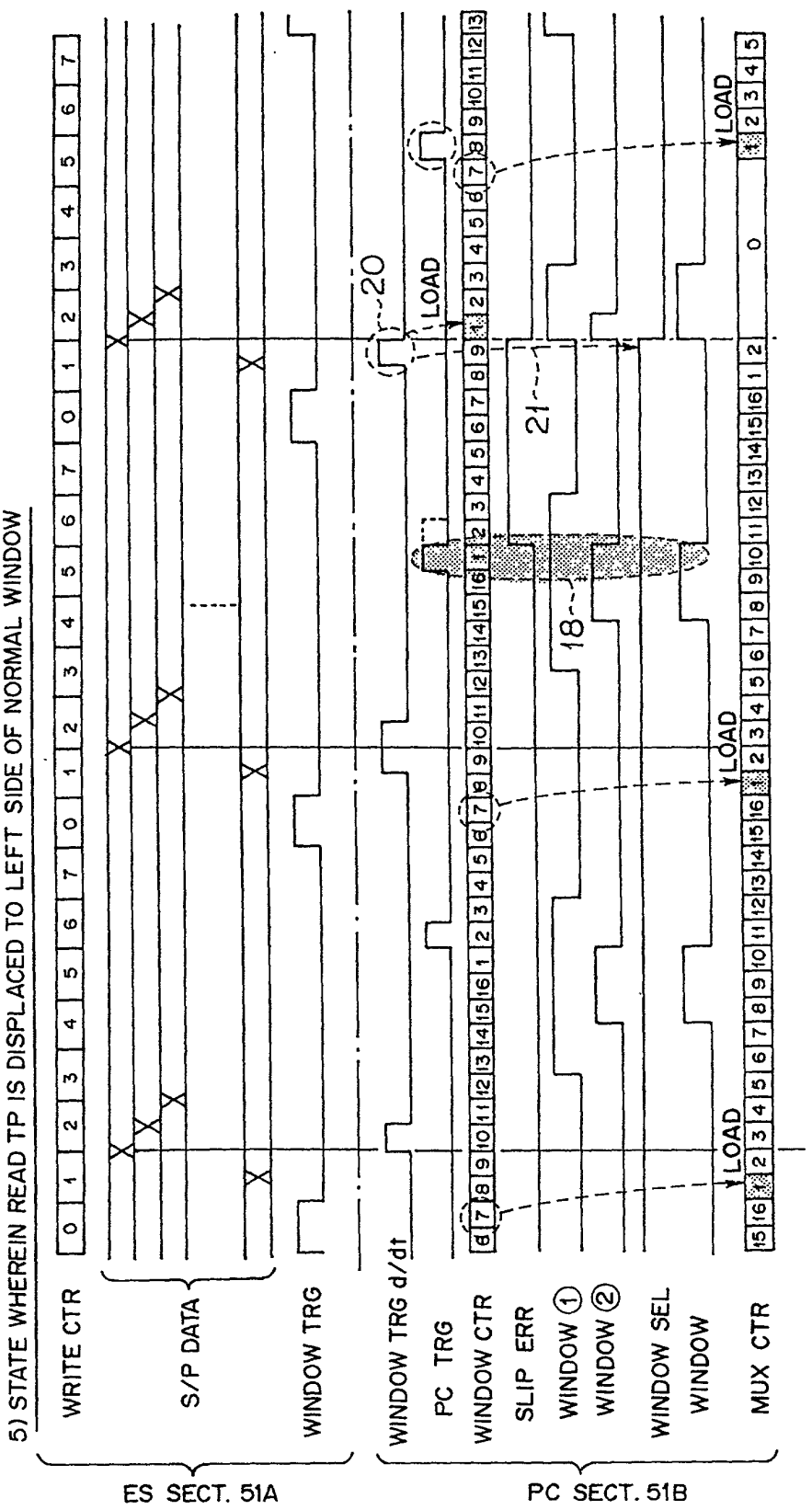


FIG. 28

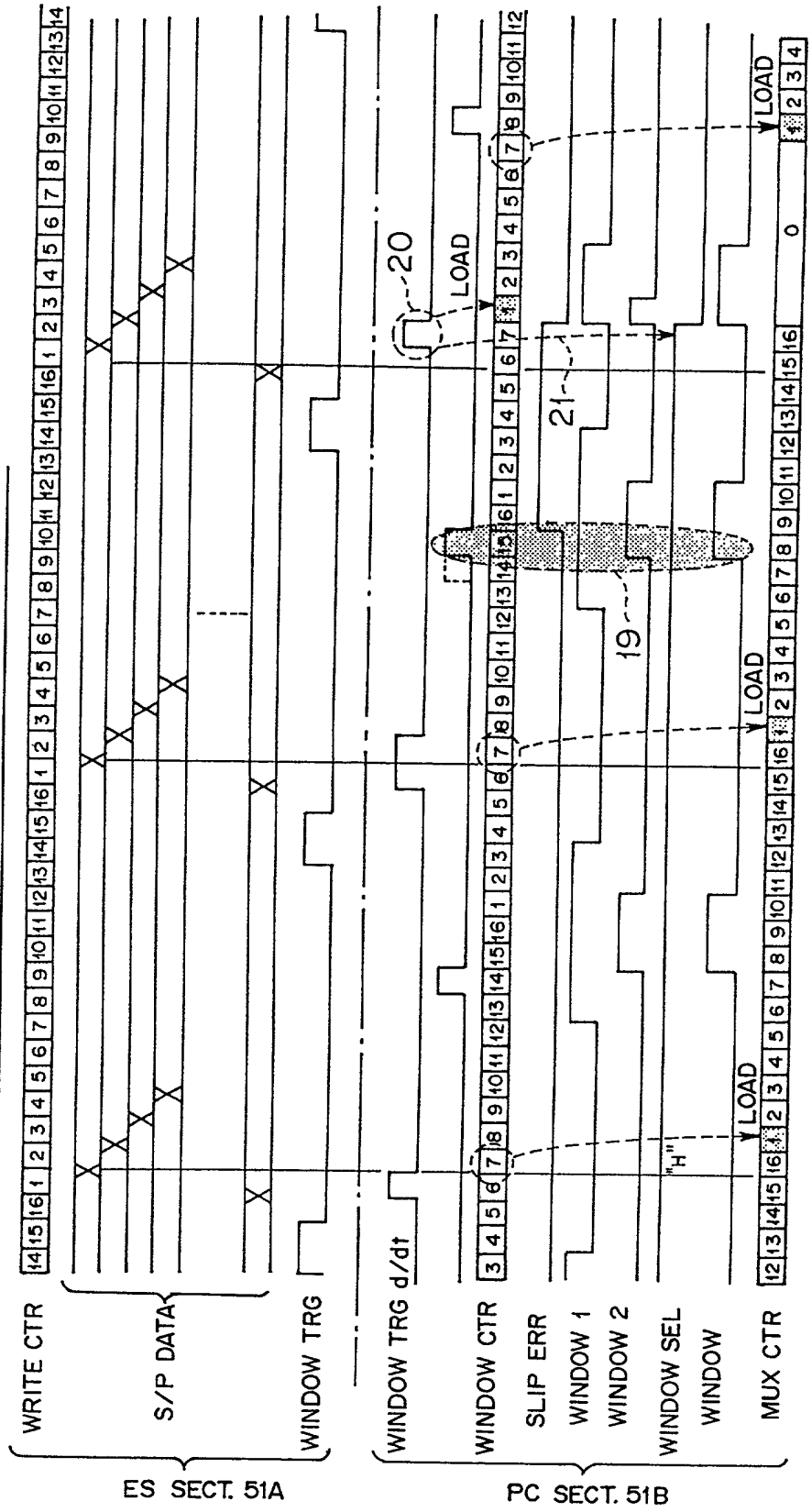


FIG. 29

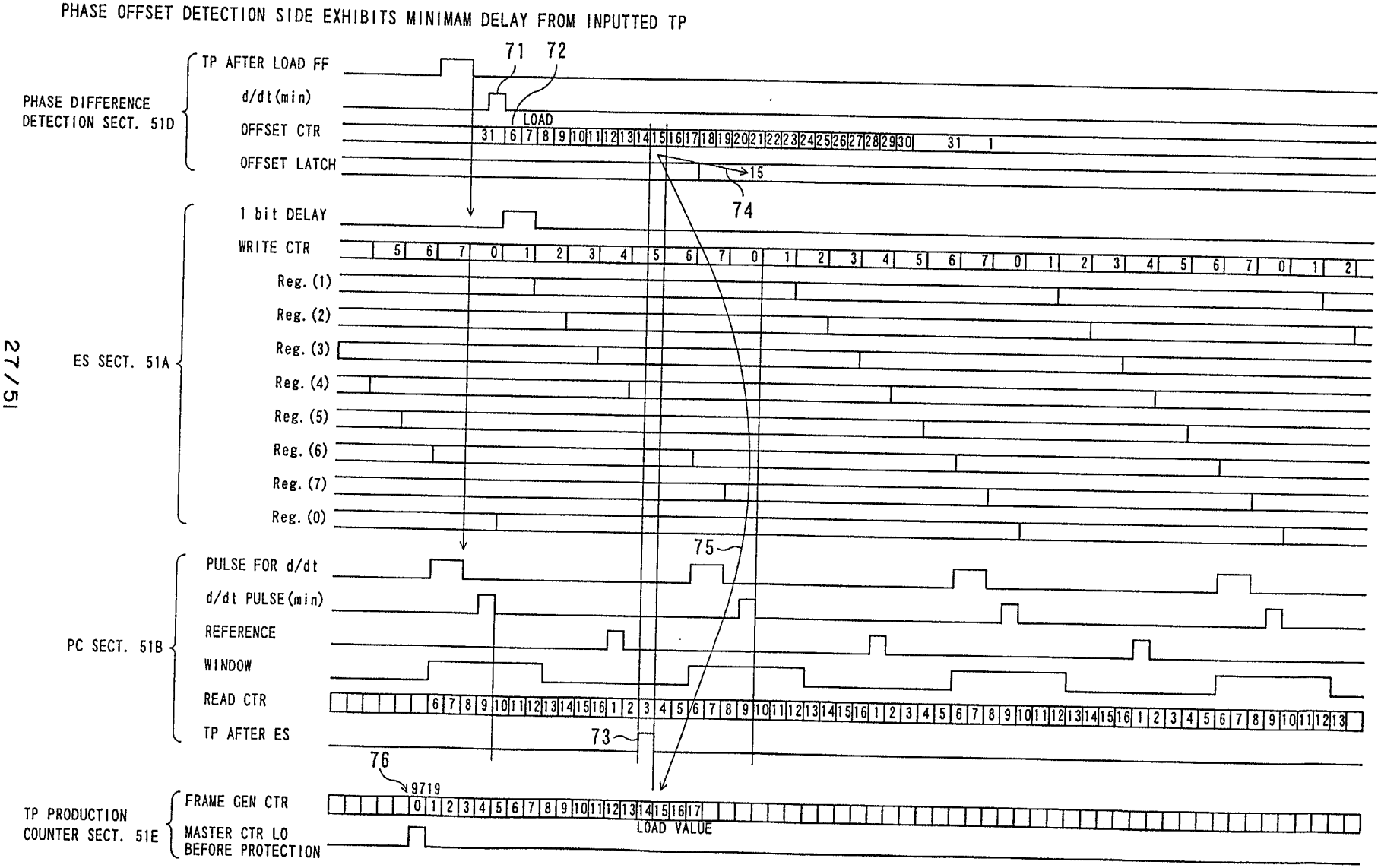


FIG. 30

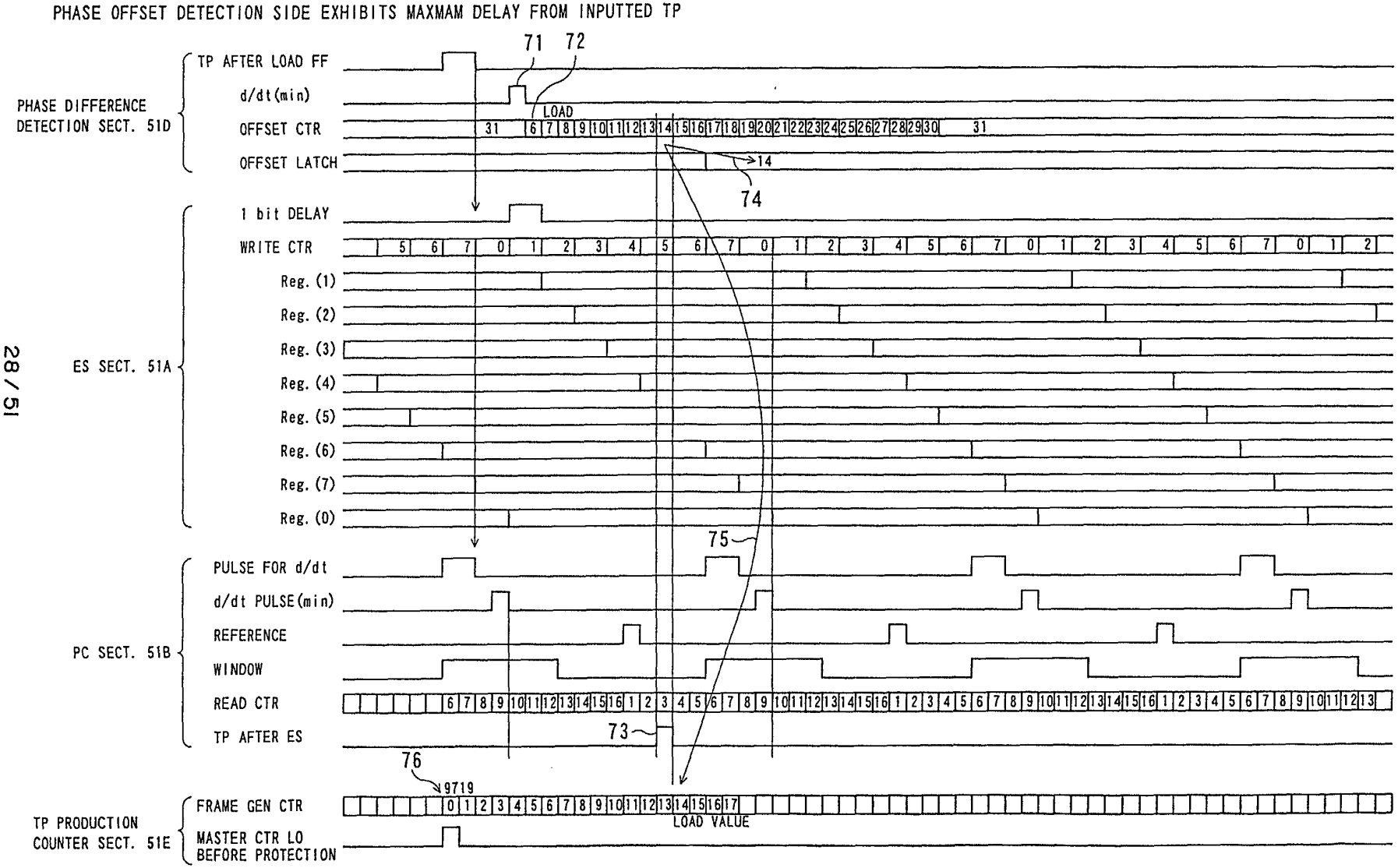


FIG. 31

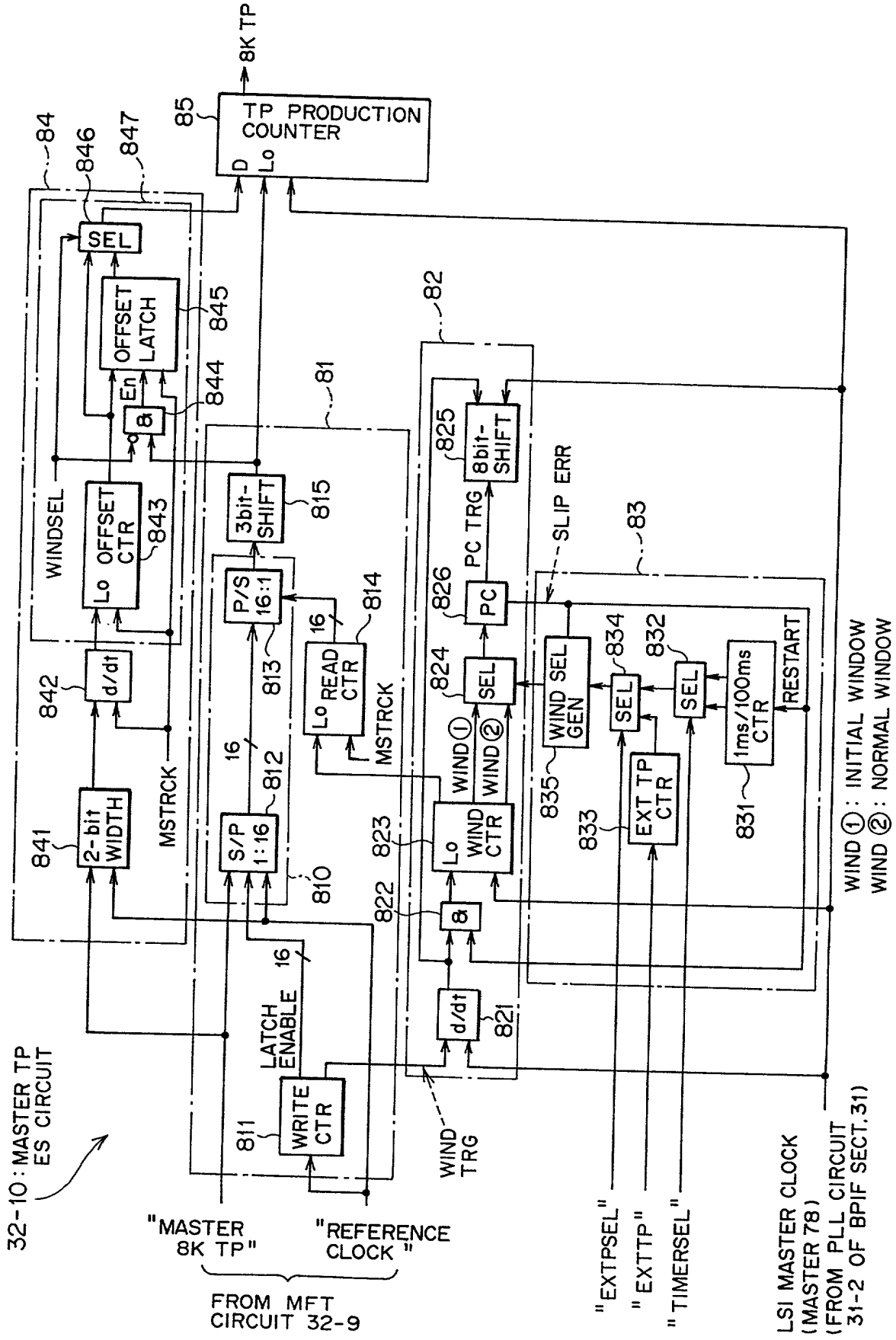


FIG. 32

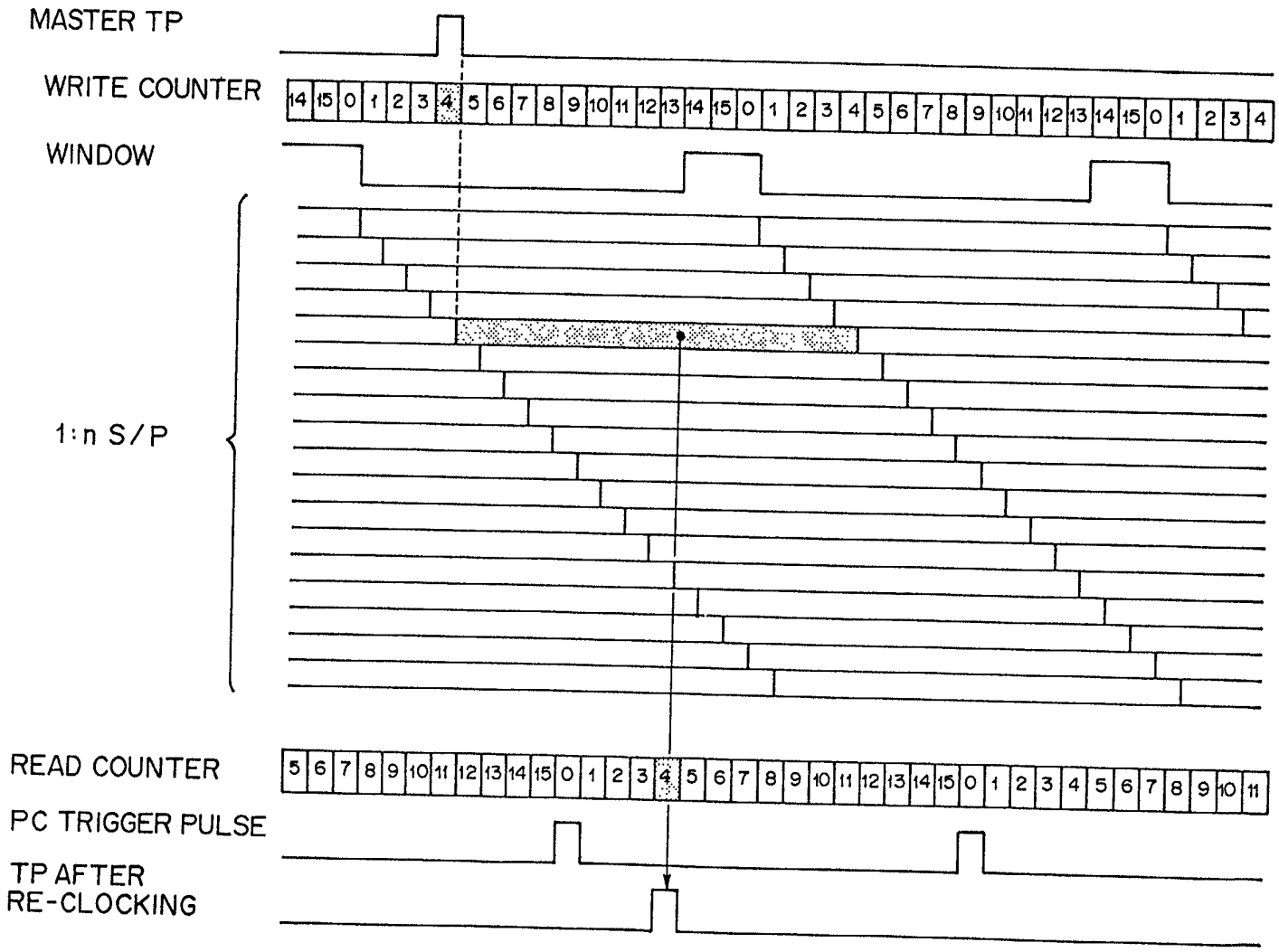

MASTER TP
WRITE COUNTER
14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4
WINDOW
1:n S/P
READ COUNTER
5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11
PC TRIGGER PULSE
TP AFTER
RE-CLOCKING

FIG. 33

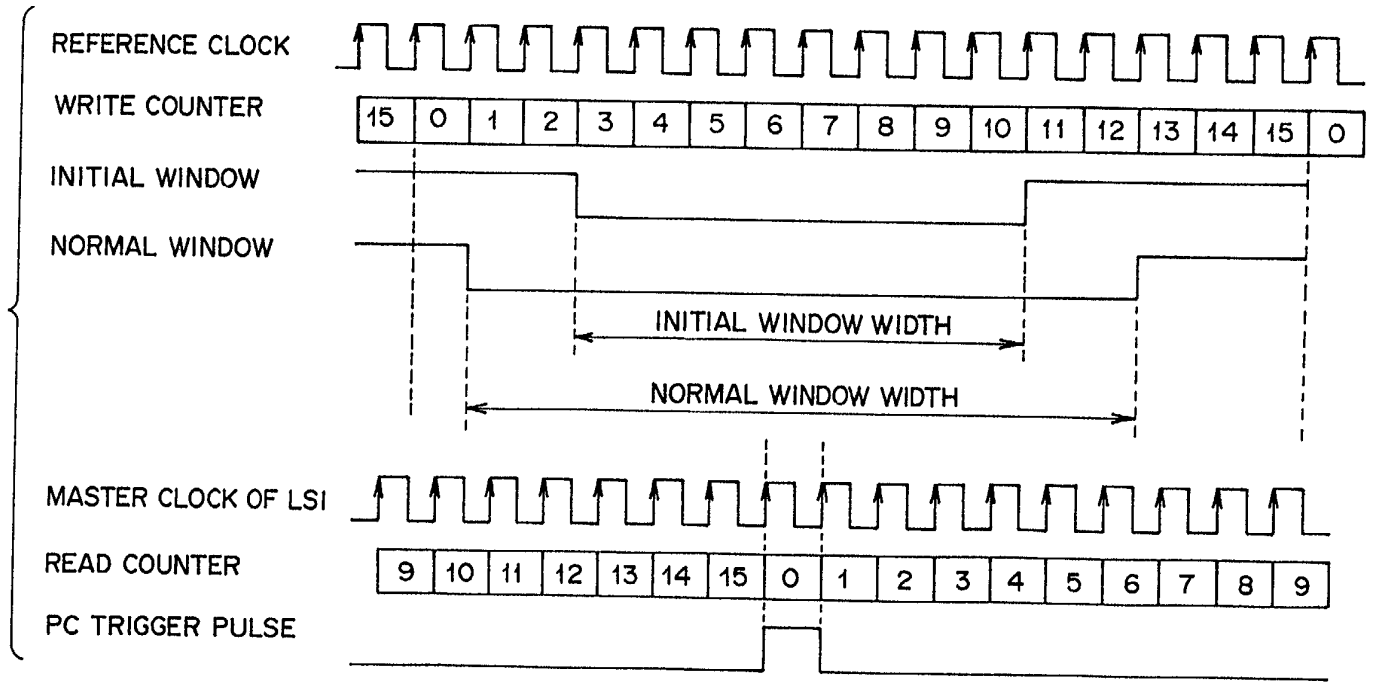


FIG. 34

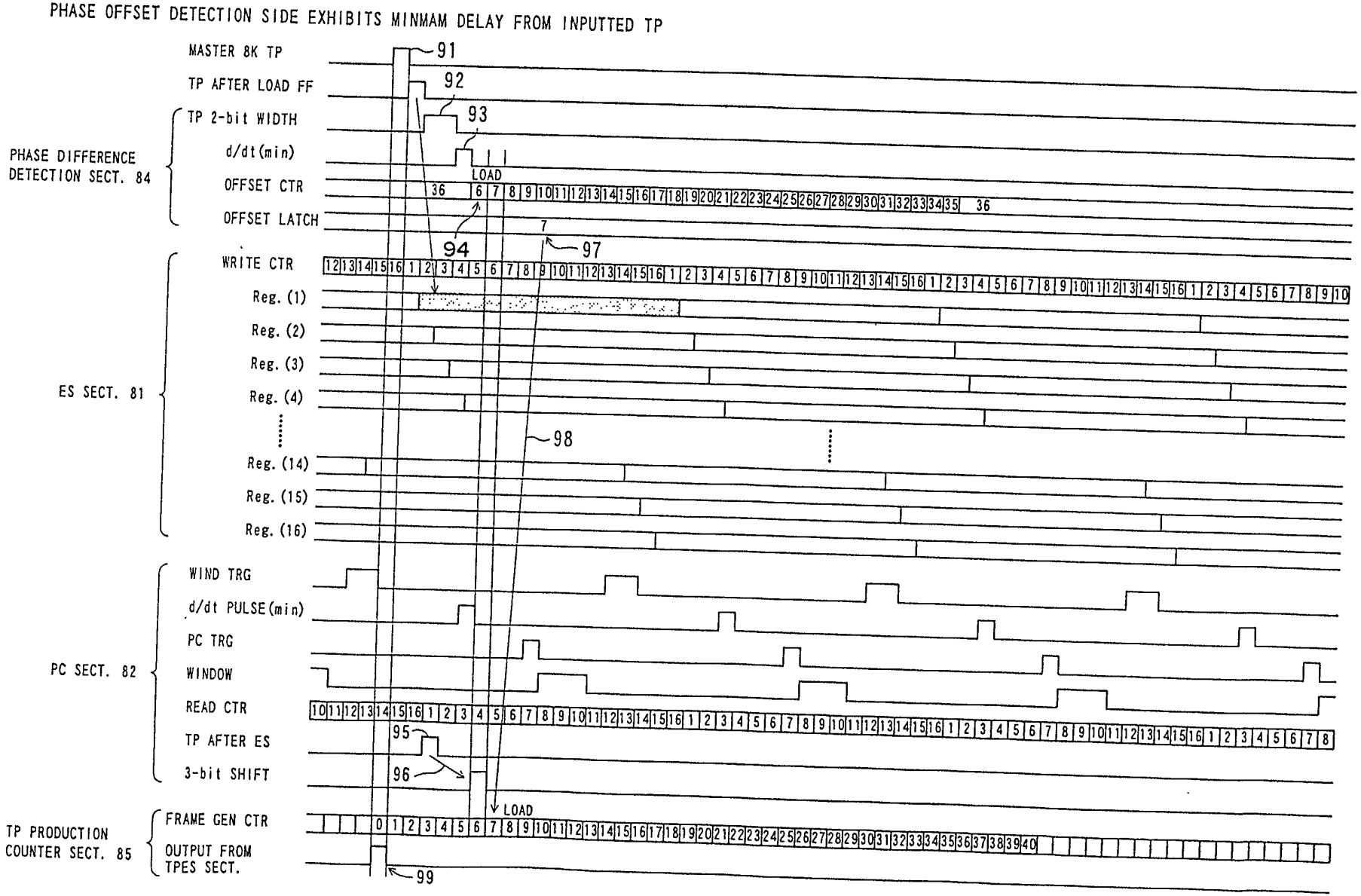

PHASE OFFSET DETECTION SIDE EXHIBITS MINMAM DELAY FROM INPUTTED TP
MASTER 8K TP
TP AFTER LOAD FF
TP 2-bit WIDTH
d/dt(min)
OFFSET CTR
OFFSET LATCH
PHASE DIFFERENCE DETECTION SECT. 84
LOAD
91
92
93
94
97
98
WRITE CTR
Reg. (1)
Reg. (2)
Reg. (3)
Reg. (4)
Reg. (14)
Reg. (15)
Reg. (16)
ES SECT. 81
WIND TRG
d/dt PULSE(min)
PC TRG
WINDOW
READ CTR
TP AFTER ES
3-bit SHIFT
PC SECT. 82
95
96
LOAD
FRAME GEN CTR
OUTPUT FROM TPES SECT.
TP PRODUCTION COUNTER SECT. 85
99

FIG. 35

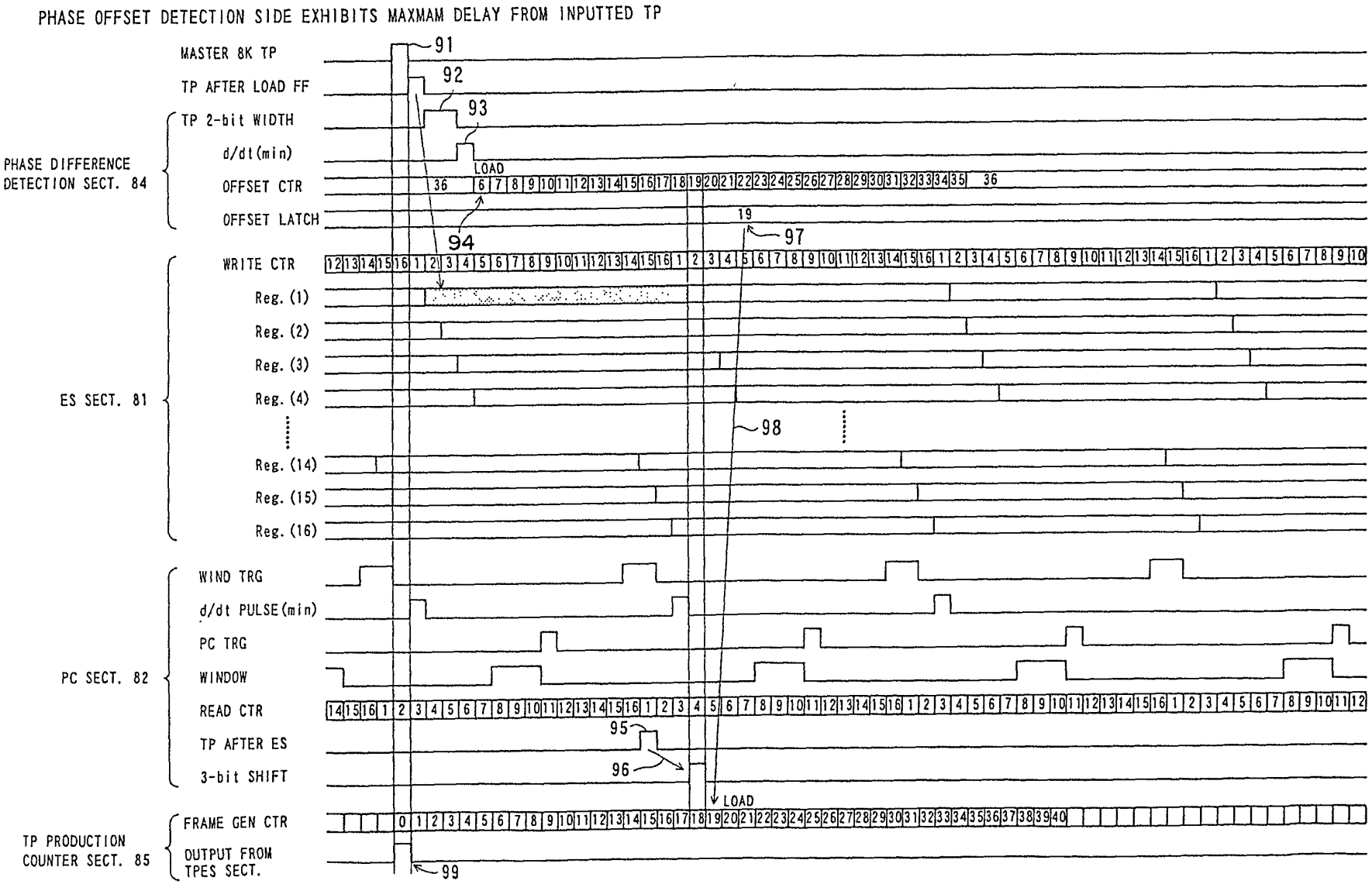

PHASE OFFSET DETECTION SIDE EXHIBITS MAXMAM DELAY FROM INPUTTED TP
MASTER 8K TP
TP AFTER LOAD FF
TP 2-bit WIDTH
d/dt(min)
OFFSET CTR
OFFSET LATCH
PHASE DIFFERENCE DETECTION SECT. 84
LOAD
WRITE CTR
Reg. (1)
Reg. (2)
Reg. (3)
Reg. (4)
Reg. (14)
Reg. (15)
Reg. (16)
ES SECT. 81
WIND TRG
d/dt PULSE(min)
PC TRG
WINDOW
READ CTR
TP AFTER ES
3-bit SHIFT
PC SECT. 82
FRAME GEN CTR
OUTPUT FROM TPES SECT.
TP PRODUCTION COUNTER SECT. 85
91
92
93
94
95
96
97
98
99

FIG. 36

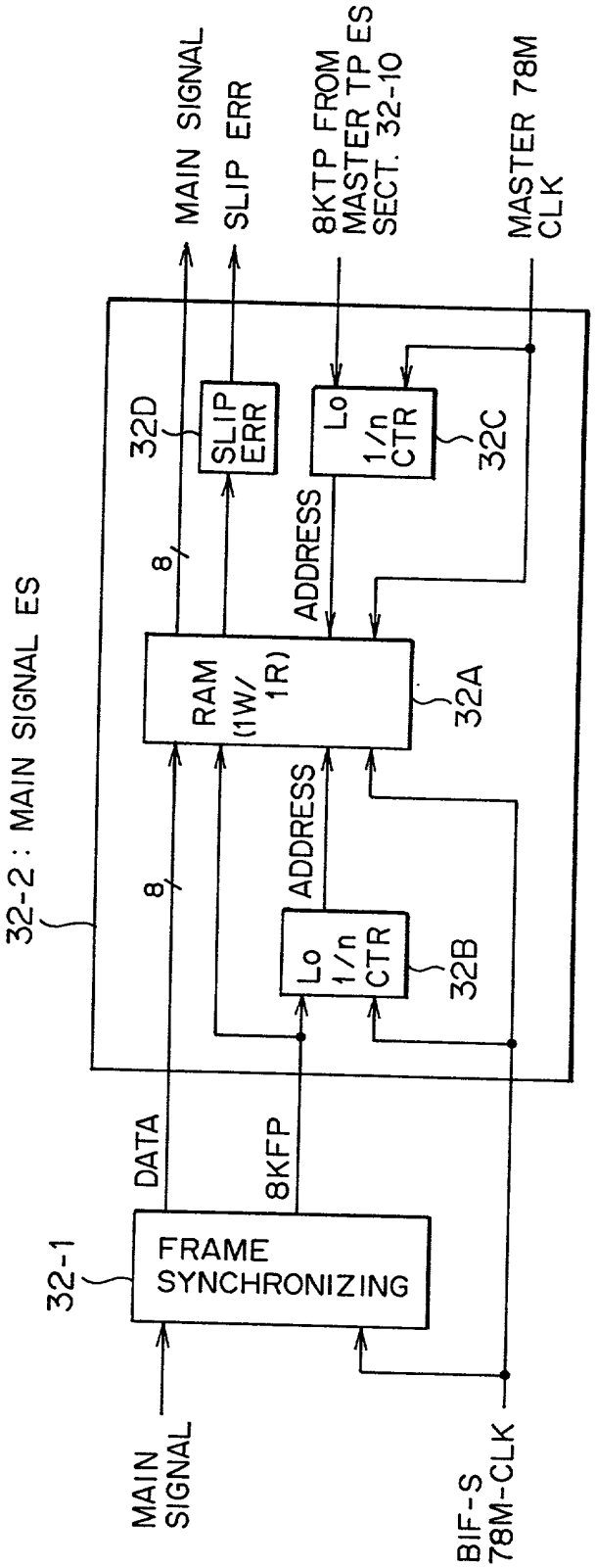


FIG. 37

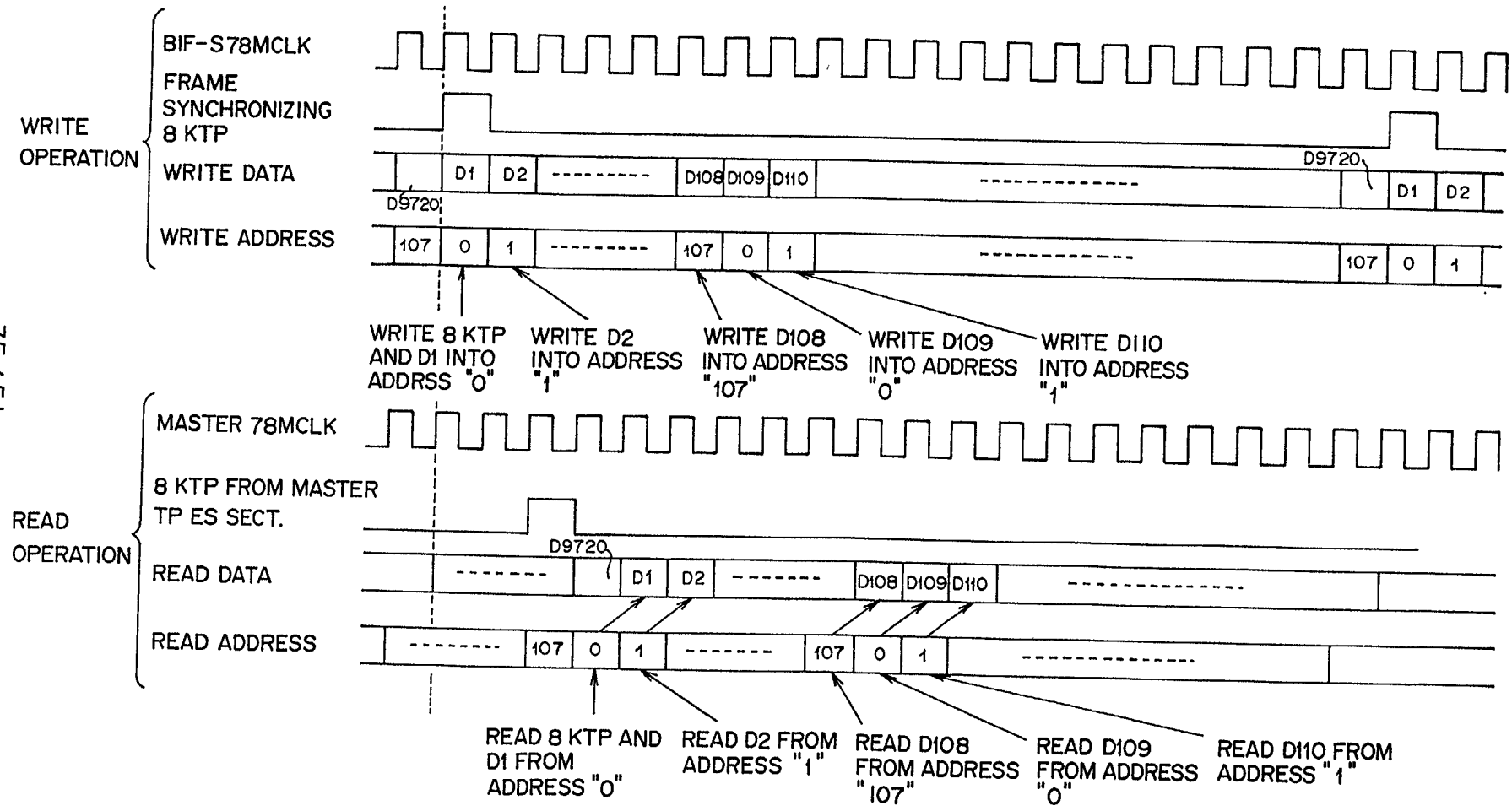
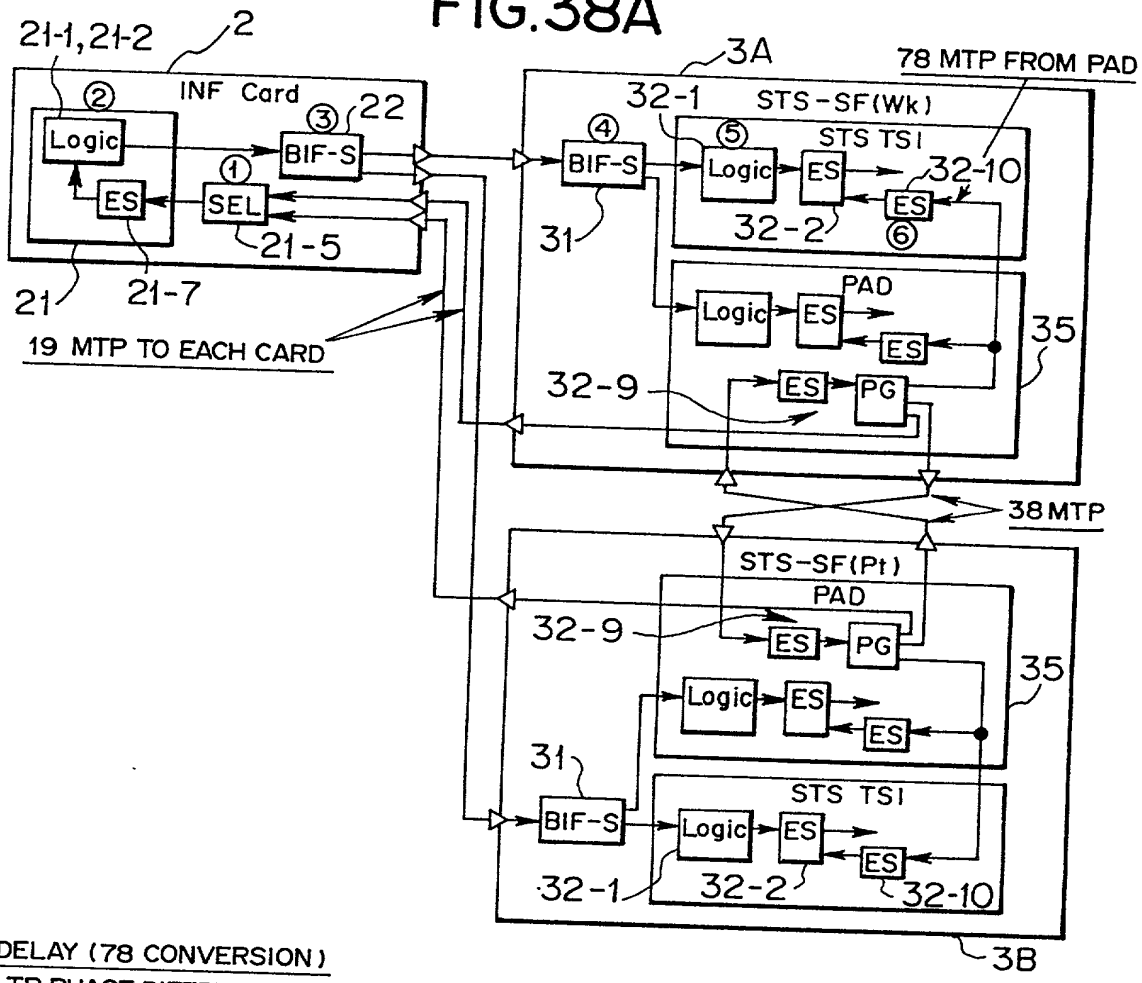

WRITE OPERATION
BIF-S78MCLK
FRAME SYNCHRONIZING 8 KTP
WRITE DATA
WRITE ADDRESS
D9720
D1
D2
D108
D109
D110
107
0
1
WRITE 8 KTP AND D1 INTO ADDRSS "0"
WRITE D2 INTO ADDRESS "1"
WRITE D108 INTO ADDRESS "107"
WRITE D109 INTO ADDRESS "0"
WRITE D110 INTO ADDRESS "1"
READ OPERATION
MASTER 78MCLK
8 KTP FROM MASTER TP ES SECT.
READ DATA
READ ADDRESS
READ 8 KTP AND D1 FROM ADDRESS "0"
READ D2 FROM ADDRESS "1"
READ D108 FROM ADDRESS "107"
READ D109 FROM ADDRESS "0"
READ D110 FROM ADDRESS "1"

FIG.38A



Bit-DELAY (78 CONVERSION)

① TP PHASE DIFFERENCE FROM STS SF WK. Pt OF INF CARD-- Min: 0ns Max: 4bits
② bit-DELAY OF CMOS LOGIC ON INF CARD ----- Min: 1ns Max: 28bits
③ MUX SIDE bit-DELAY OF BIF-SLSI ON INF CARD ----- Min: 22.5bits Max: 39.5bits
④ DMUX SIDE bit-DELAY OF BIF-SLSI ON STS-SF CARD --- Min: 4.875bits Max: 6.875bits
⑤ LOGIC DELAY OF STS TSI LSI ----- Min: 4bits Max: 14bits

TOTAL Min: 31.375bits Max: 92.375bits

FIG.38B

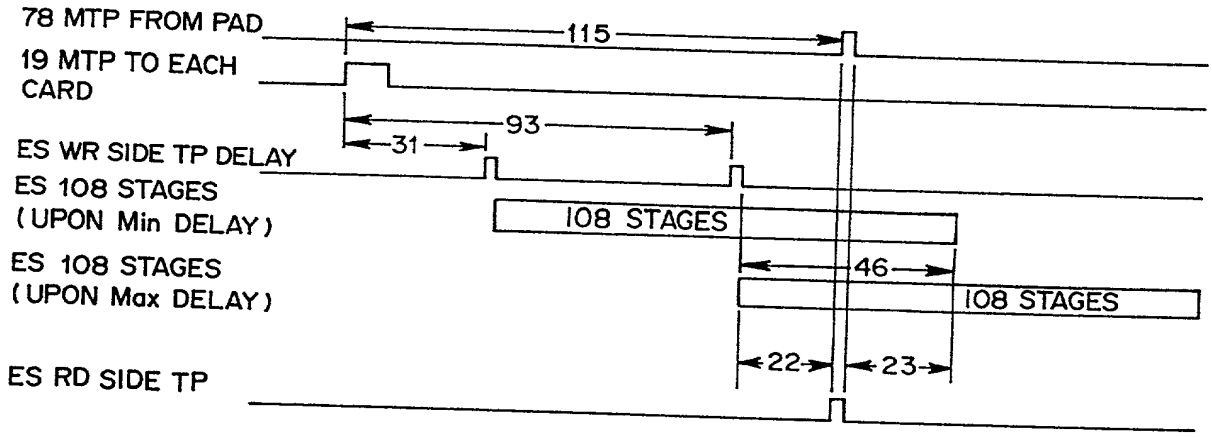


FIG. 39

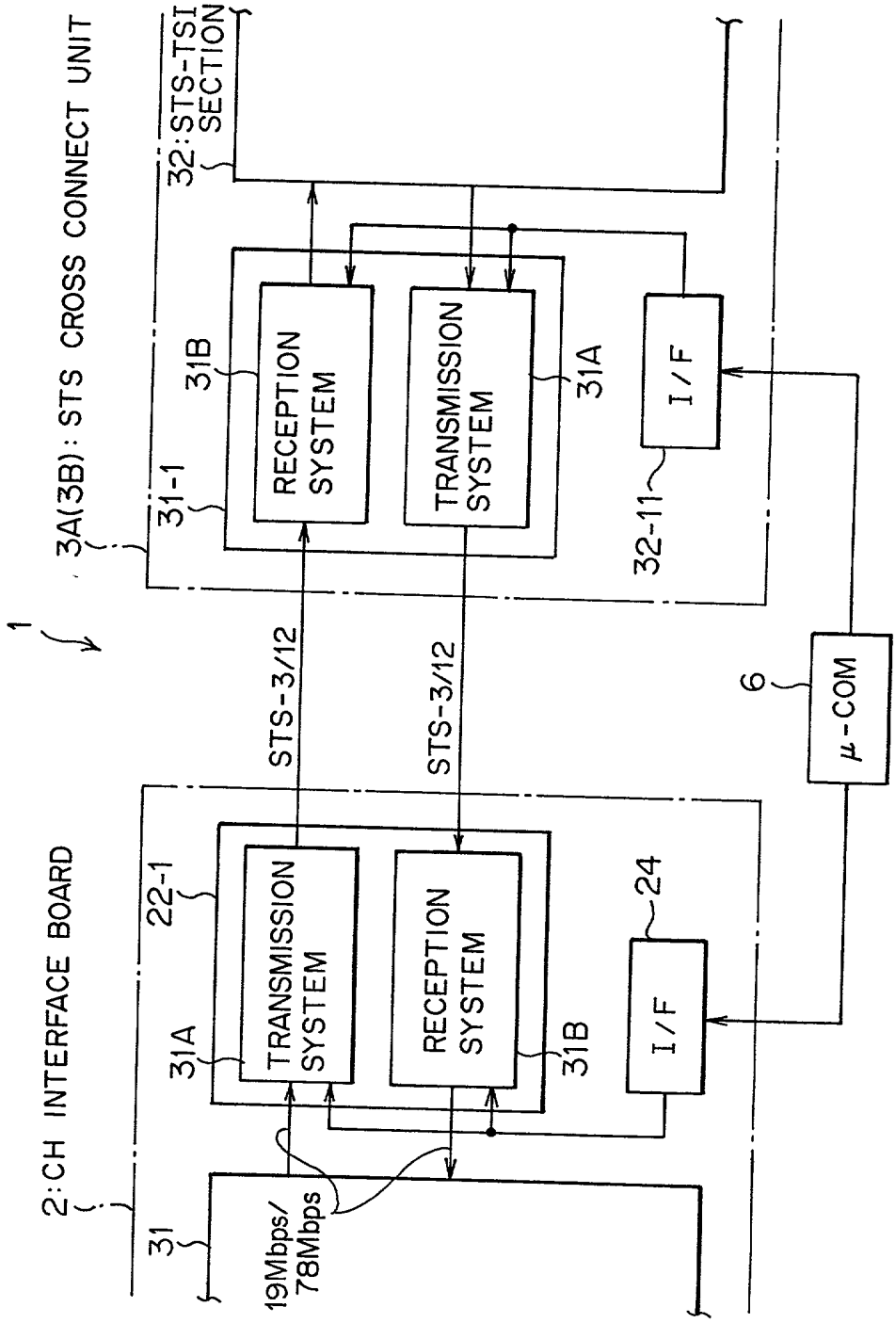


FIG. 40A

BANDWIDTH	① → ② → ③ → ④	OPERATION MODE
0	19.44M→19.44M→155.52M→155.52M	OPERATION MODE A
1	77.76M→77.76M→155.52M→622.08M	OPERATION MODE B

FIG. 40B

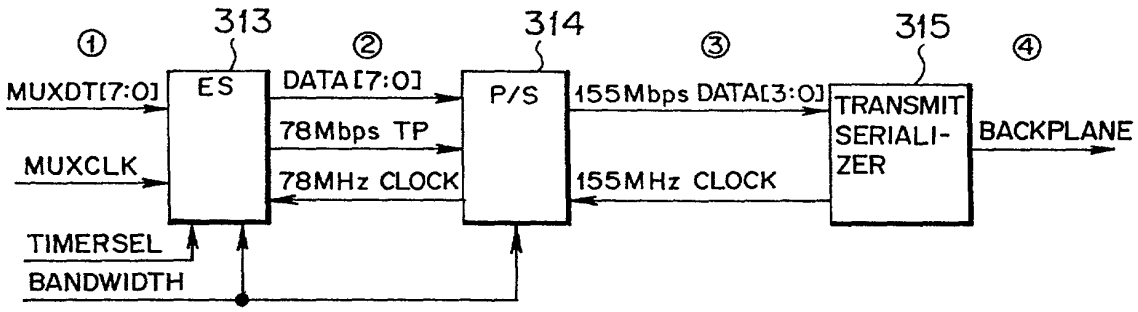


FIG. 41

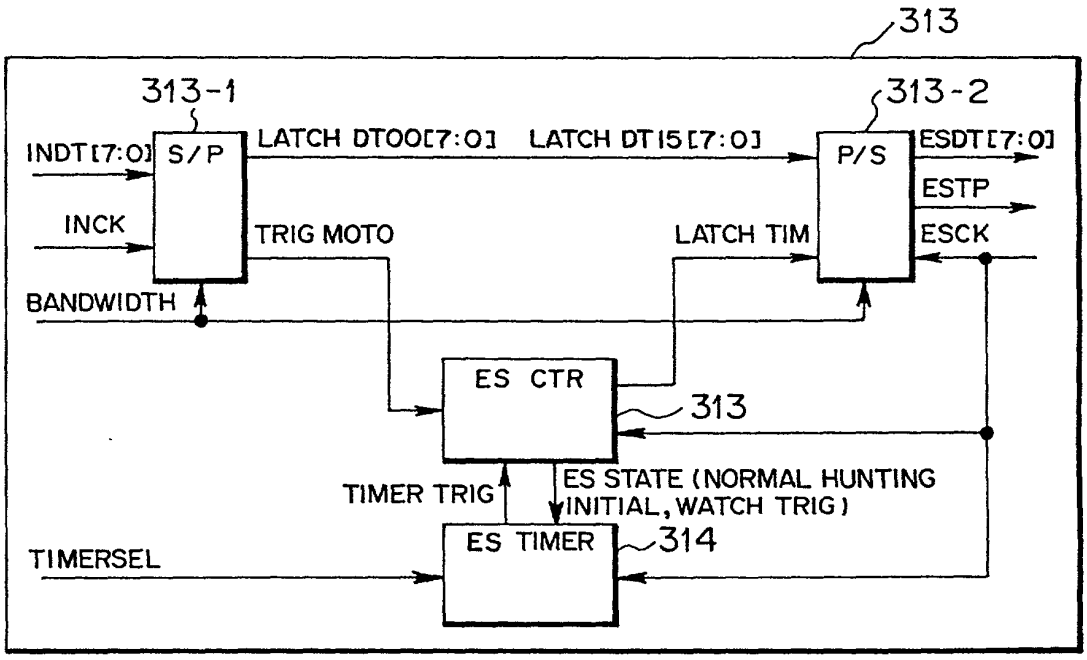

313
313-1
313-2
INDT[7:0]
S/P
LATCH DT00[7:0]
LATCH DT15[7:0]
P/S
ESDT[7:0]
ESTP
INCK
TRIG MOTO
LATCH TIM
ESCK
BANDWIDTH
ES CTR
313
TIMER TRIG
ES STATE (NORMAL HUNTING
INITIAL, WATCH TRIG)
ES TIMER
314
TIMERSEL

FIG.42

TRANSMISSION SIDE FORMAT CONVERSION

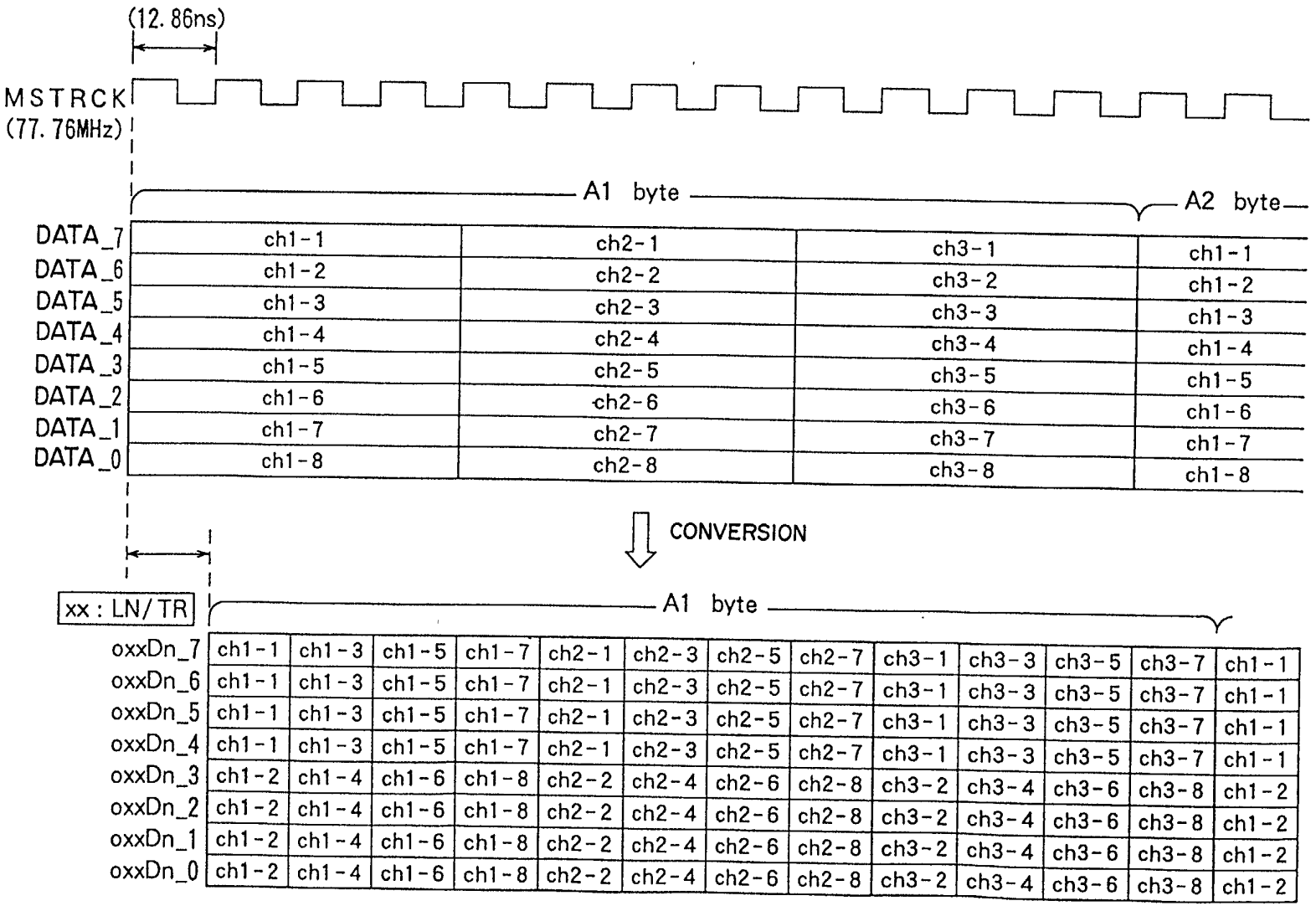


FIG. 43A

BANDWIDTH	①→②→③	OPERATION MODE
0	155.52M→155.52M→19.44M	OPERATION MODE A
1	622.08M→155.52M→77.76M	OPERATION MODE B
1	155.52M→155.52M→77.76M	OPERATION MODE C

FIG. 43B

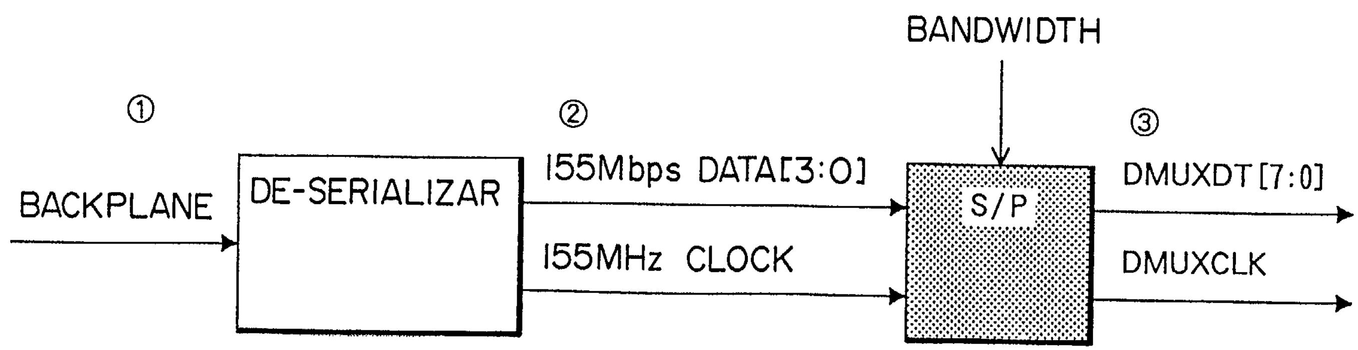


FIG. 44

RECEPTION SIDE FORMAT CONVERSION

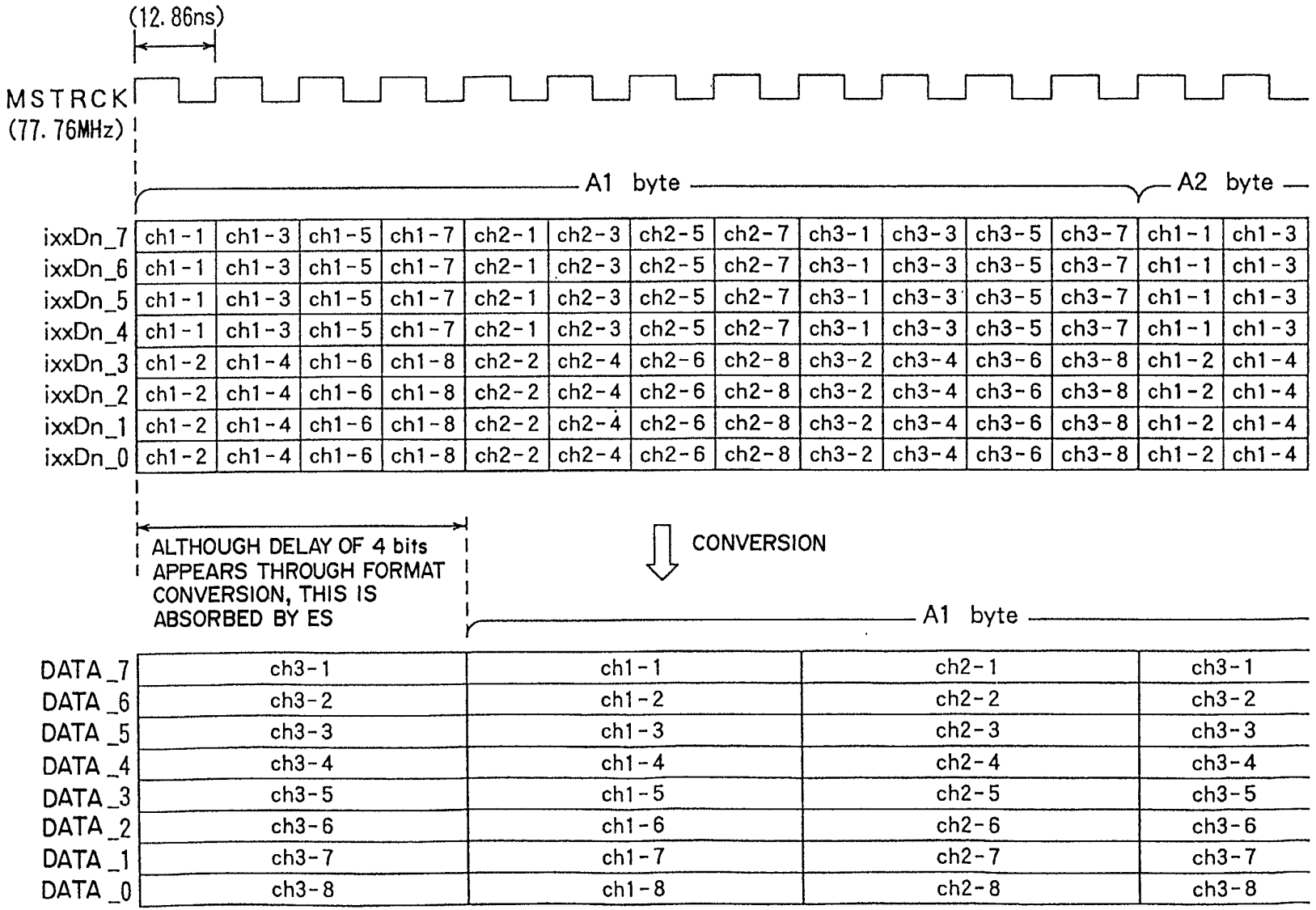


FIG. 45

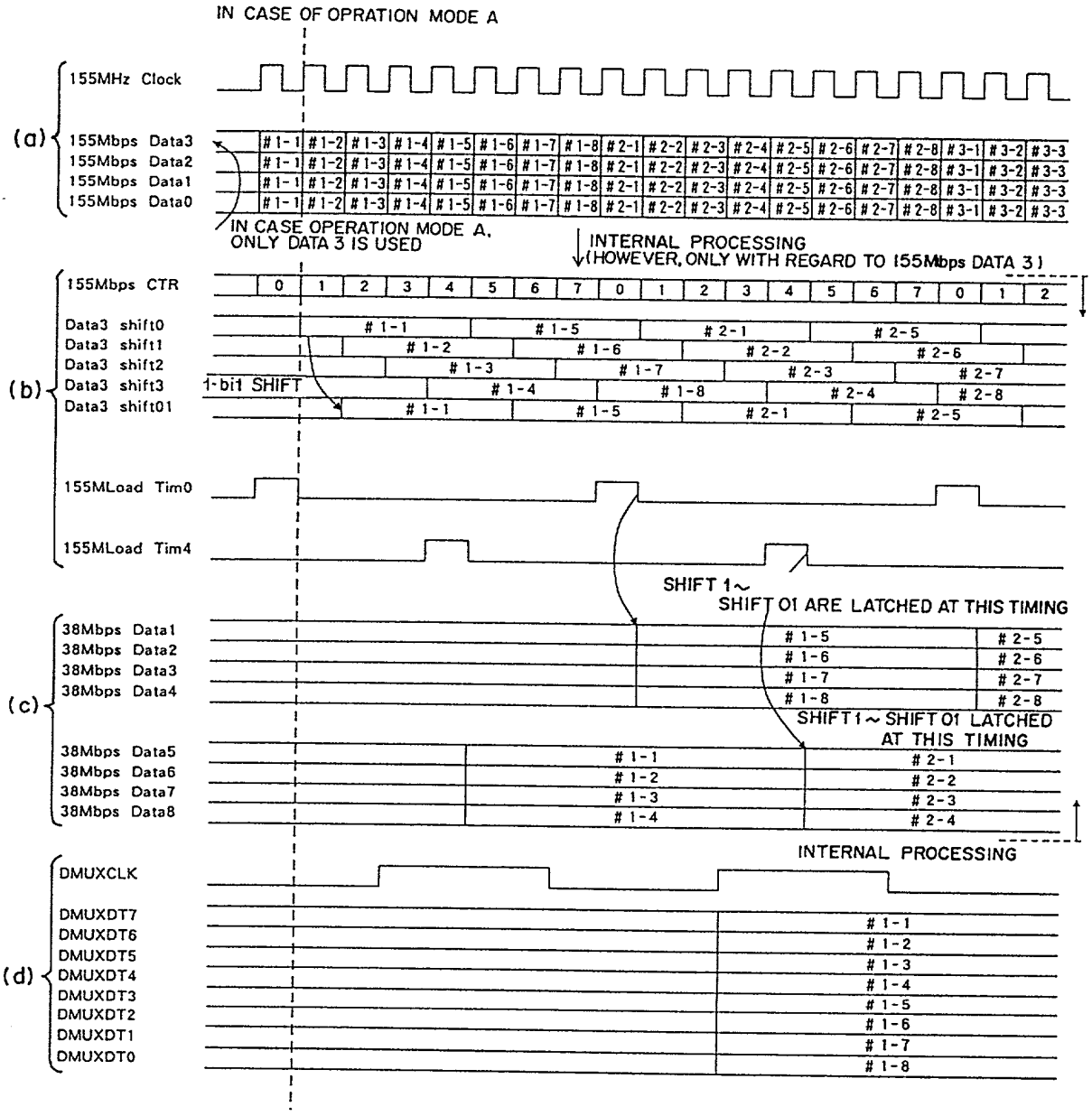

IN CASE OF OPRATION MODE A
155MHz Clock
(a)
155Mbps Data3
155Mbps Data2
155Mbps Data1
155Mbps Data0
IN CASE OPERATION MODE A, ONLY DATA 3 IS USED
INTERNAL PROCESSING (HOWEVER, ONLY WITH REGARD TO 155Mbps DATA 3)
155Mbps CTR
Data3 shift0
Data3 shift1
Data3 shift2
Data3 shift3
Data3 shift01
(b)
1-bit SHIFT
155MLoad Tim0
155MLoad Tim4
SHIFT 1~ SHIFT 01 ARE LATCHED AT THIS TIMING
38Mbps Data1
38Mbps Data2
38Mbps Data3
38Mbps Data4
(c)
38Mbps Data5
38Mbps Data6
38Mbps Data7
38Mbps Data8
SHIFT 1~ SHIFT 01 LATCHED AT THIS TIMING
INTERNAL PROCESSING
DMUXCLK
DMUXDT7
DMUXDT6
DMUXDT5
DMUXDT4
DMUXDT3
DMUXDT2
DMUXDT1
DMUXDT0
(d)

FIG. 46

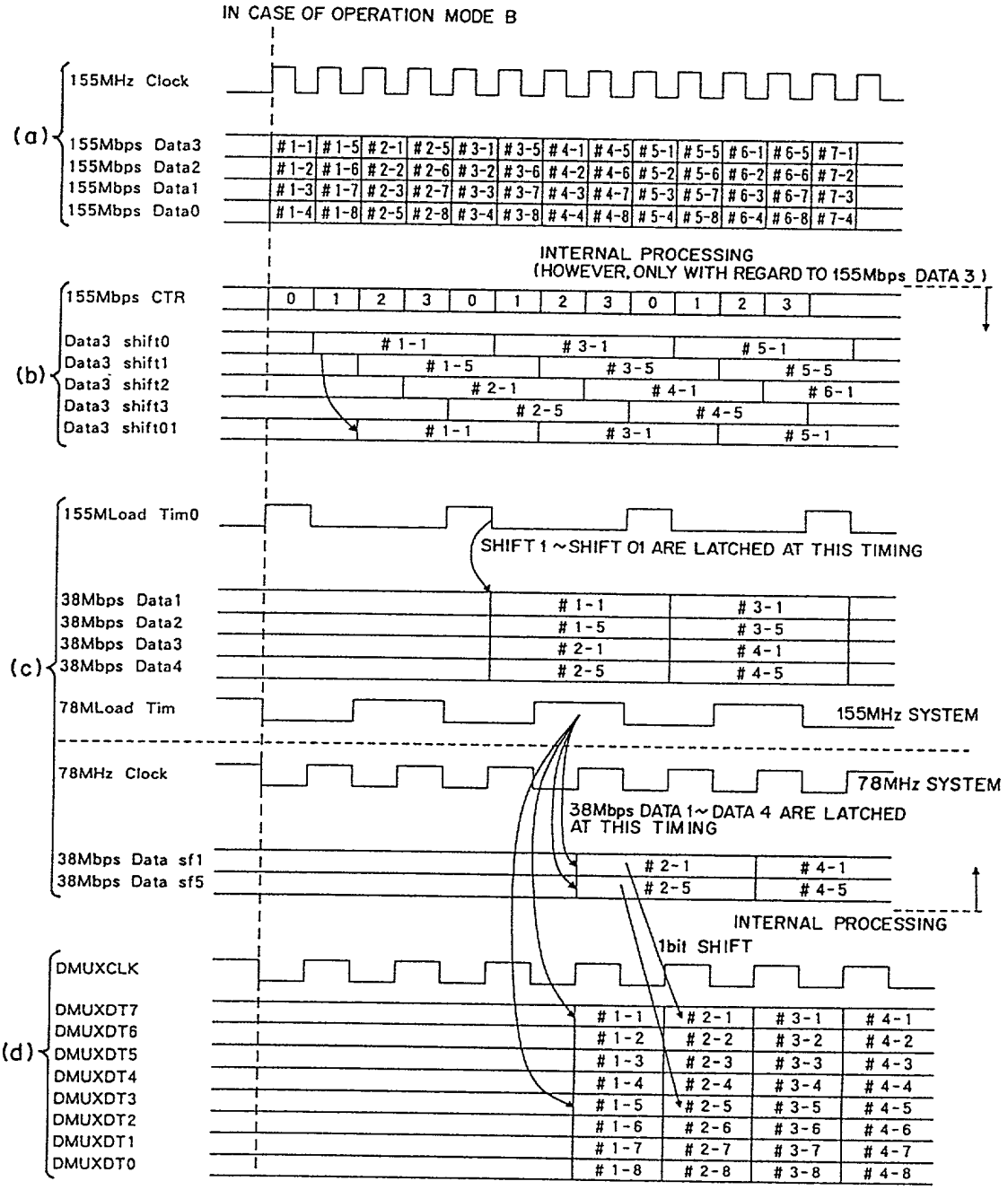

IN CASE OF OPERATION MODE B
(a)
155MHz Clock
155Mbps Data3
155Mbps Data2
155Mbps Data1
155Mbps Data0
INTERNAL PROCESSING
(HOWEVER, ONLY WITH REGARD TO 155Mbps DATA 3)
(b)
155Mbps CTR
Data3 shift0
Data3 shift1
Data3 shift2
Data3 shift3
Data3 shift01
(c)
155MLoad Tim0
SHIFT 1 ~ SHIFT 01 ARE LATCHED AT THIS TIMING
38Mbps Data1
38Mbps Data2
38Mbps Data3
38Mbps Data4
78MLoad Tim
155MHz SYSTEM
78MHz Clock
78MHz SYSTEM
38Mbps DATA 1 ~ DATA 4 ARE LATCHED AT THIS TIMING
38Mbps Data sf1
38Mbps Data sf5
INTERNAL PROCESSING
1bit SHIFT
(d)
DMUXCLK
DMUXDT7
DMUXDT6
DMUXDT5
DMUXDT4
DMUXDT3
DMUXDT2
DMUXDT1
DMUXDT0

FIG. 47

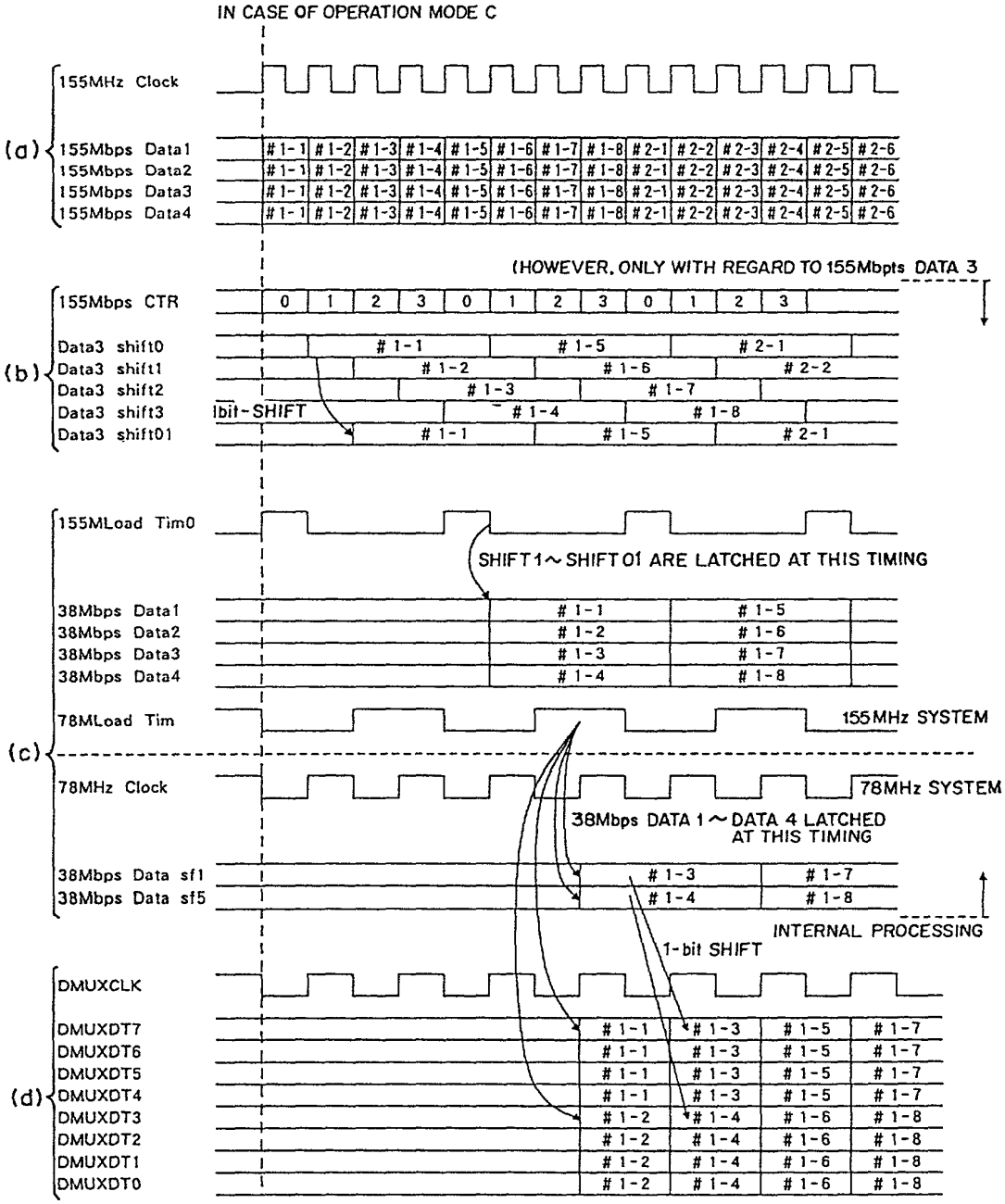


FIG.48

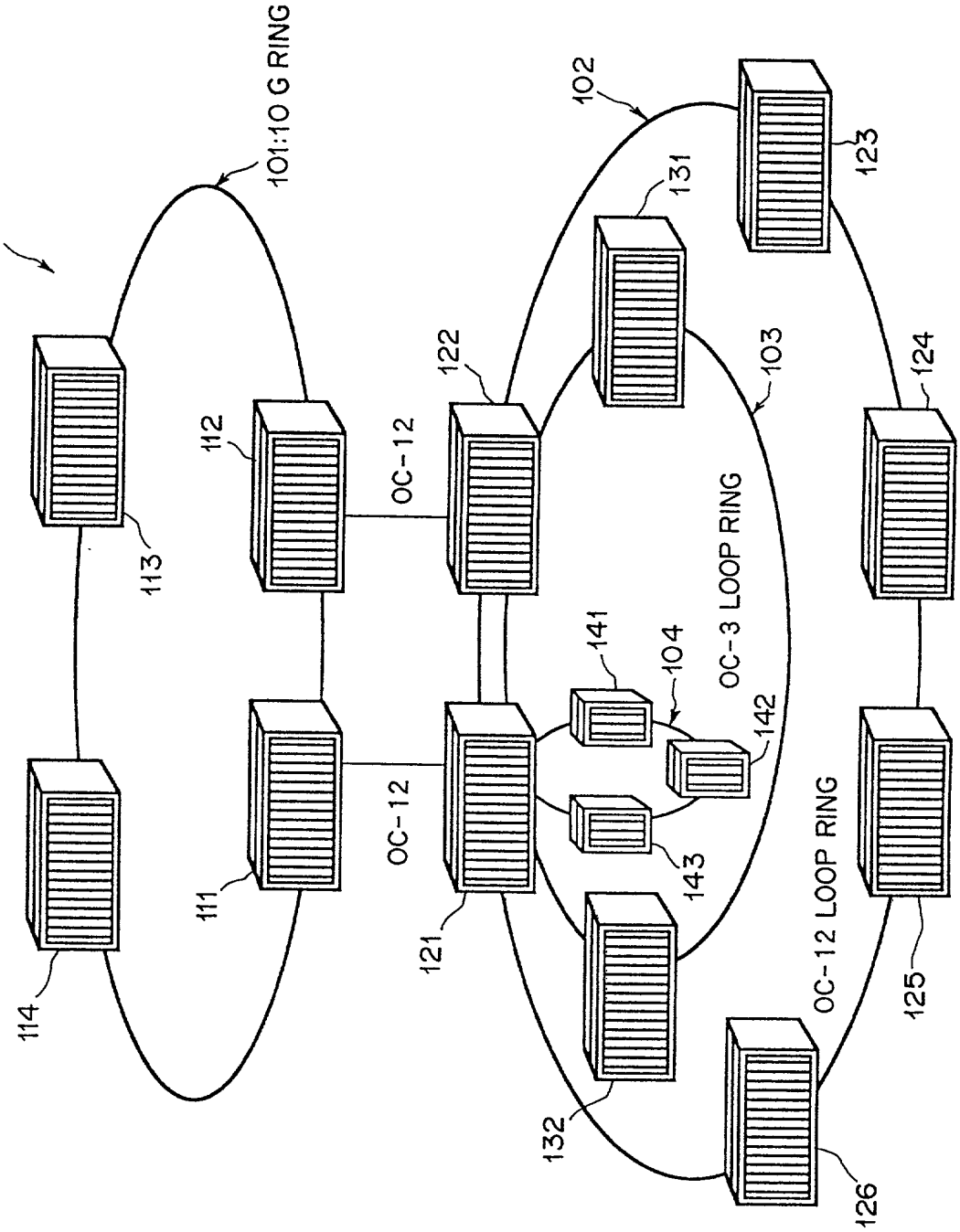


FIG.49

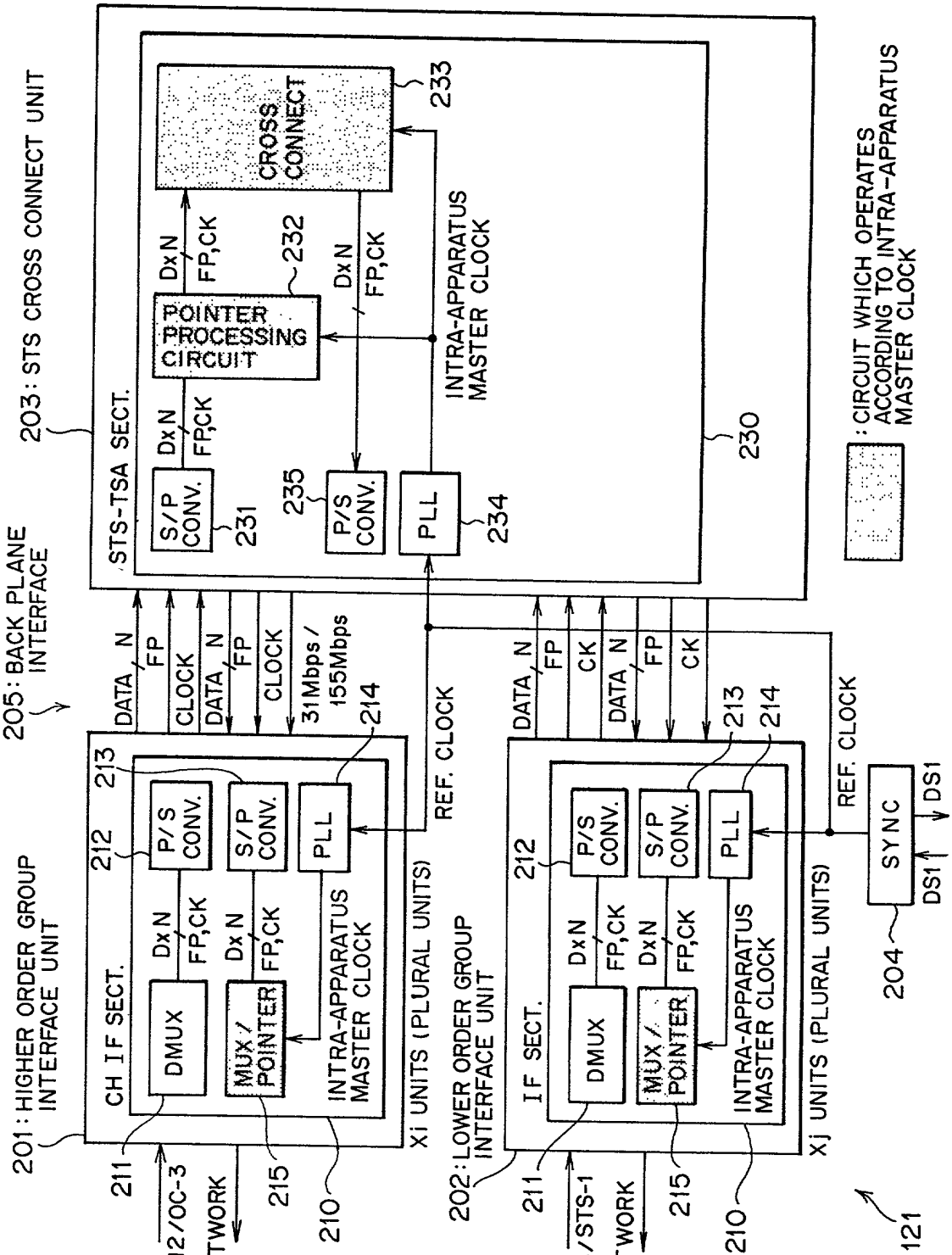


FIG. 50

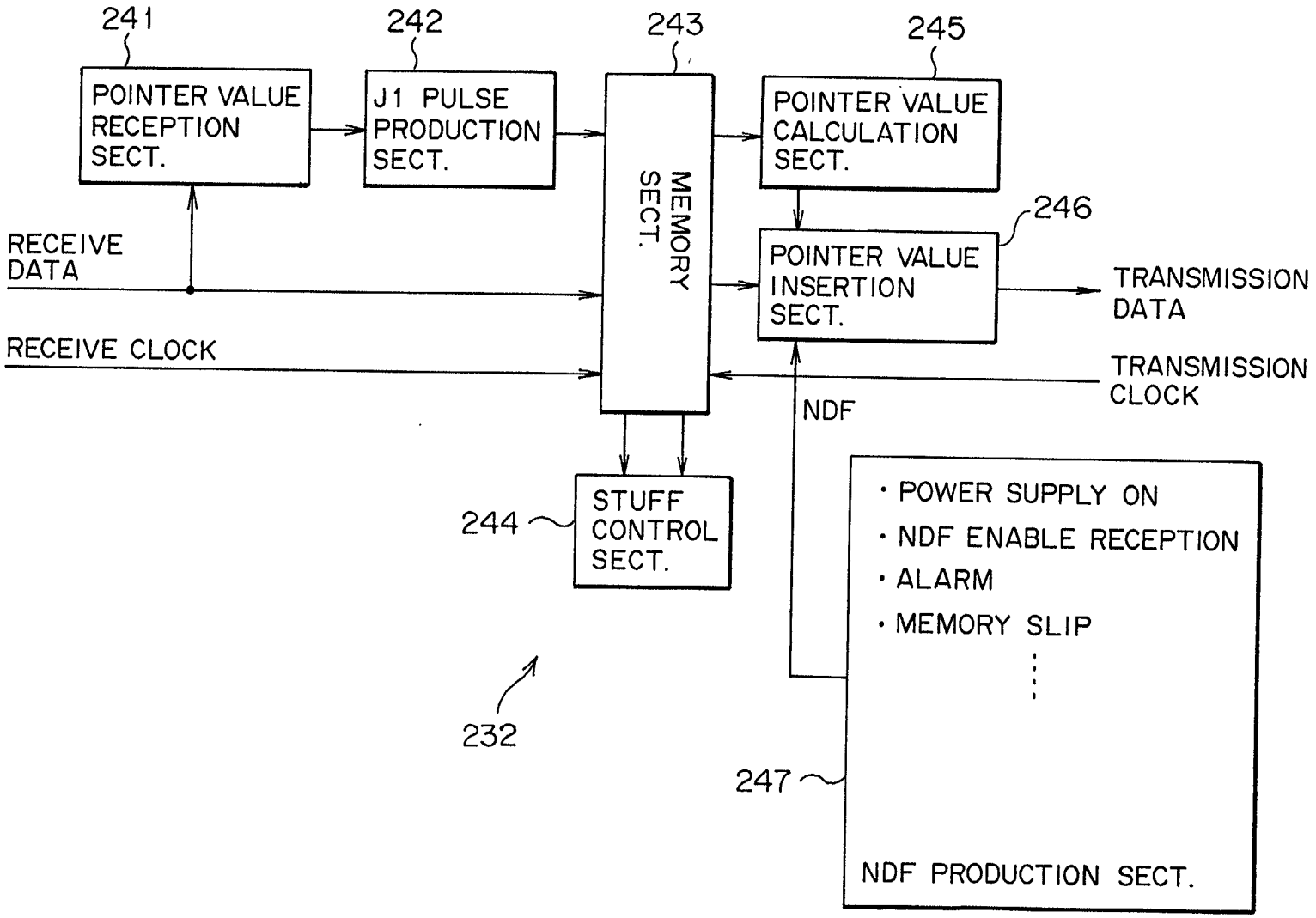

241
242
243
245
POINTER VALUE RECEPTION SECT.
J1 PULSE PRODUCTION SECT.
MEMORY SECT.
POINTER VALUE CALCULATION SECT.
246
POINTER VALUE INSERTION SECT.
RECEIVE DATA
RECEIVE CLOCK
TRANSMISSION DATA
TRANSMISSION CLOCK
NDF
244
STUFF CONTROL SECT.
232
247
• POWER SUPPLY ON
• NDF ENABLE RECEPTION
• ALARM
• MEMORY SLIP
NDF PRODUCTION SECT.

FIG. 51

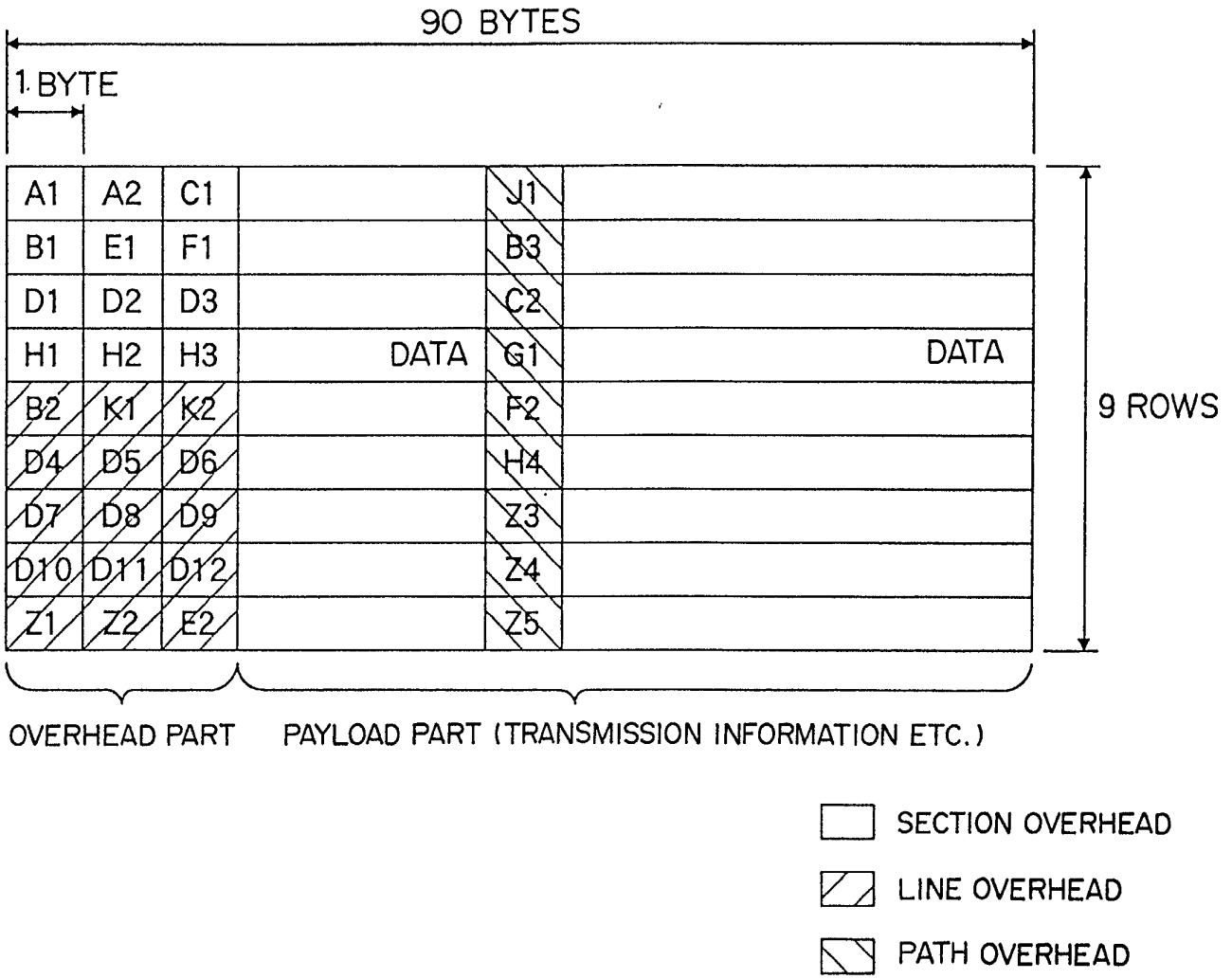


FIG. 52

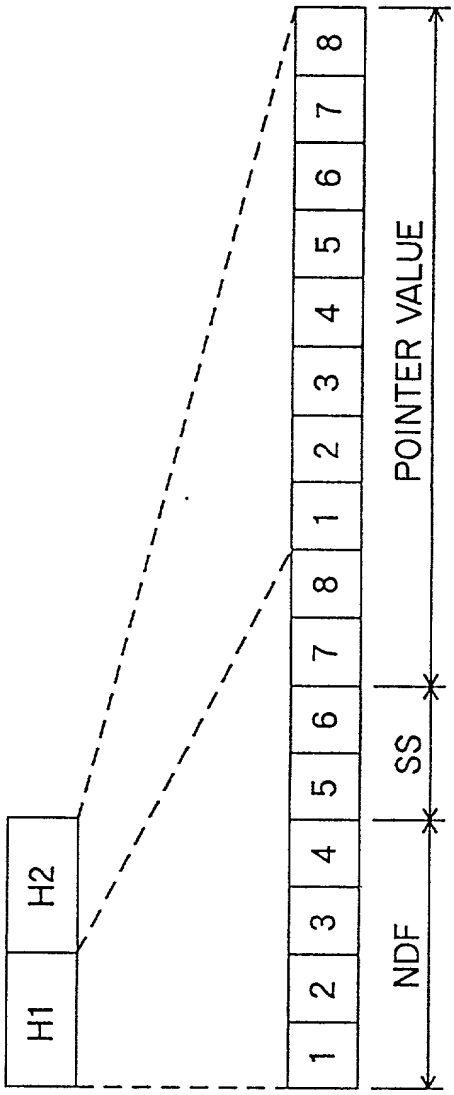


FIG. 53

	1	2	3	4	5	6	7	8	9	89	90
1	A1	A2	C1	522							608
2	B1	E1	F1	609							695
3	D1	D2	D3	696							782
4	H1	H2	H3	0	1	2	3	4	5	85	86
5	B2	K1	K2	87							173
6	D4	D5	D6	174							260
7	D7	D8	D9	261							347
8	D10	D11	D12	348							434
9	Z1	Z2	E2	435							521